CALIFORNIA INSTITUTE OF TECHNOLOGY
PHYSICS MATHEMATICS AND ASTRONOMY DIVISION

Sophomore Physics Laboratory

Physics 5 and 105 Course Laboratory Notes

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Chapter 1

Resonant Circuits

1.1 Introduction

Resonators, one of the most useful and used device, are essentially physical systems that present a more or less pronounced peak in their transfer function.

In general, their performance is measured by a dimensionless parameter named quality factor Q, which characterizes the sharpness of the resonant peak. The higher the quality factor the sharper is the peak and the better is the resonator.

Quite often, the major issues of building a resonator are to obtain very high quality factors and good stability. For example, mechanical oscillators made of fused silica fibers under load, can achieve quality factors above 10^8 in the acoustic band[**?**]. Very high quality factors in electronics can be achieved using the mechanical resonances of piezoelectric materials such as quartz. Lasers and resonant cavities made of mirrors can be used to build resonators in the optical frequency range. The same principle can be applied in the microwave range. Thermal stabilization is always a key ingredient to obtain high stability.

Resonators made with electronic passive components, reaching quality factors values up to 10-100 or more, are quite easy to realize. In the next sections we will study two typical resonant circuits, the LCR series and LCR parallel circuits.

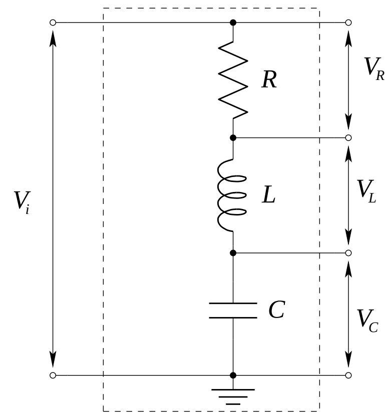


Figure 1.1: LCR series circuit.

1.2 The LCR Series Resonant Circuit

Figure 1.1 shows the so called *LCR series resonant circuit*. Depending on voltage difference, we are considering as the circuit output (the capacitor, the resistor, or the inductor), this circuit shows a different behavior. Let's study indeed in the frequency and in the domain, the response of this passive circuit for each one of the possible non trivial outputs.

1.2.1 Frequency Response with Capacitor Voltage Difference as Circuit Output

Considering the voltage difference V_C across the capacitor the circuit output, we will have

$$\begin{aligned} V_{in} &= \left(R + j\omega L + \frac{1}{j\omega C}\right) I, \\ V_C &= \frac{1}{j\omega C} I\,, \end{aligned}$$

and the transfer function will be

$$H_C(\omega) = \frac{1}{j\omega RC - \omega^2 LC + 1}.$$

For sake of simplicity it is convenient to define the two following quantities

$$\omega_0^2 = \frac{1}{LC}, \qquad Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \omega_0 \frac{L}{R}$$

The parameter Q is the quality factor of the circuit, and the angular frequency ω_0 is the resonant frequency of the circuit if $R = 0$.

Considering the previous definitions, and after some algebra, $H_C(\omega)$ becomes

$$H_C(\omega) = \frac{\omega_0^2}{\omega_0^2 - \omega^2 + j\omega\frac{\omega_0}{Q}} . \tag{1.1}$$

Computing the magnitude and phase of $H_C(\omega)$, we obtain

$$\begin{aligned} |H_C(\omega)| &= \frac{\omega_0^2}{\sqrt{\left(\omega_0^2 - \omega^2\right)^2 + \left(\omega\frac{\omega_0}{Q}\right)^2}} , \\ \arg\left[H_C(\omega)\right] &= -\arctan\left(\frac{1}{Q}\frac{\omega_0\omega}{\omega_0^2 - \omega^2}\right) . \end{aligned}$$

The magnitude has maximum for

$$\omega_C^2 = \omega_0^2\left(1 - \frac{1}{2Q^2}\right) ,$$

and the maximum is

$$|H_C(\omega_C)| = \frac{Q}{\sqrt{1 - \frac{1}{4Q^2}}} .$$

If $Q \gg 1$ then $\omega_C \simeq \omega_0$, and $|H_C(\omega_C)| \simeq Q$.

Far from resonance ω_C, the approximate behavior of $|H_C(\omega)|$ is

$$\begin{aligned} \omega \ll \omega_C \quad &\Rightarrow \quad |H_C(\omega)| \simeq 1 , \\ \omega \gg \omega_C \quad &\Rightarrow \quad |H_C(\omega)| \simeq \frac{\omega_0^2}{\omega^2} . \end{aligned}$$

Figure 1.2 shows the magnitude and phase of $H_C(\omega)$. In this case the circuit is a low pass filter of the second order because of the asymptotic slope $1/\omega^2$.

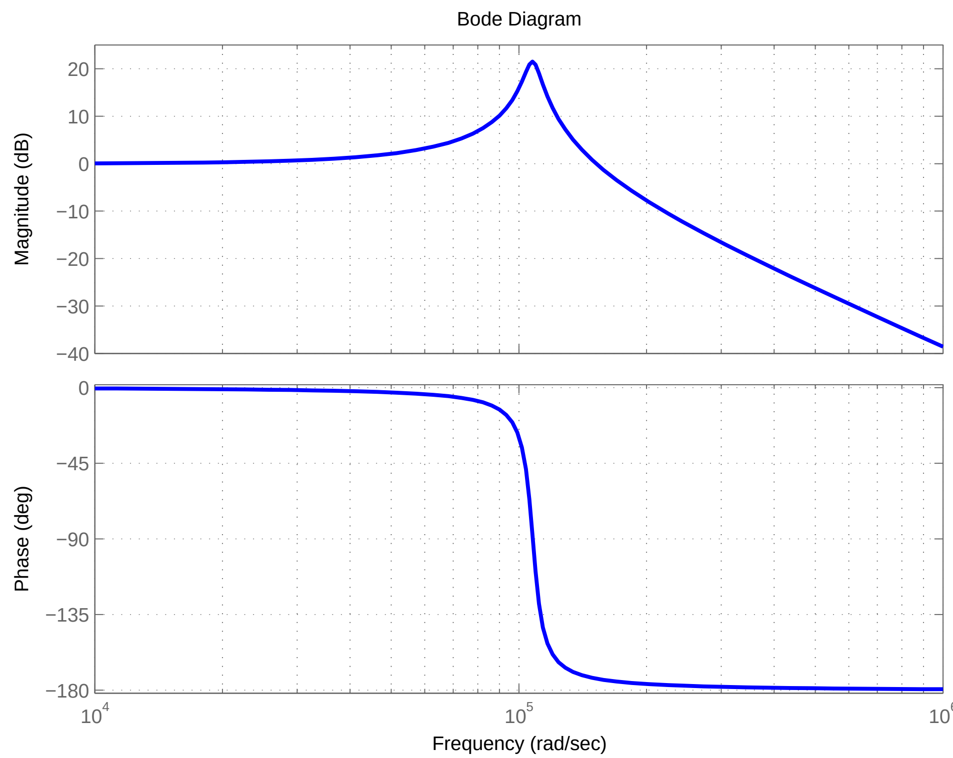


Figure 1.2: Transfer function $H_C(\omega)$ of the LCR series resonant circuit with a resonant angular frequency $\omega_C \simeq 10.7$krad/s.

1.2.2 Frequency Response with Inductor Voltage Difference as Circuit Output

Considering the voltage difference V_L across the inductor as the circuit output, we will have instead

$$H_L(\omega) = -\frac{\omega^2 LC}{j\omega RC - \omega^2 LC + 1}.$$

Using the definition of Q, and ω_0 and after some algebra, $H_L(\omega)$ becomes

$$H_L(\omega) = \frac{-\omega^2}{\omega_0^2 - \omega^2 + j\omega\frac{\omega_0}{Q}} \tag{1.2}$$

Computing the magnitude and phase of $H_L(\omega)$, we obtain

$$\begin{aligned} |H_L(\omega)| &= \frac{\omega^2}{\sqrt{\left(\omega_0^2 - \omega^2\right)^2 + \left(\omega\frac{\omega_0}{Q}\right)^2}} \\ \arg\left[H_L(\omega)\right] &= \arctan\left(\frac{1}{Q}\frac{\omega\omega_0}{\omega_0^2 - \omega^2}\right) \end{aligned}$$

The magnitude has a maximum for

$$\omega_L^2 = \omega_0^2 \frac{1}{1 - \frac{1}{2Q^2}},$$

and the maximum is

$$|H_L(\omega_L)| = \frac{Q}{\sqrt{1 - \frac{1}{4Q^2}}}.$$

If $Q \gg 1$ then $\omega_L \simeq \omega_0$, and $|H_L(\omega_L)| \simeq Q$.
Far from resonance ω_L, the approximate behavior of $|H_L(\omega)|$ is

$$\begin{aligned} \omega &\ll \omega_L \quad \Rightarrow \quad |H_L(\omega)| \simeq \frac{\omega^2}{\omega_0^2} \\ \omega &\gg \omega_L \quad \Rightarrow \quad |H_L(\omega)| \simeq 1 \end{aligned}$$

Figure 1.3 shows the magnitude and phase of $H_L(\omega)$. In this case the circuit is a second order high pass filter.

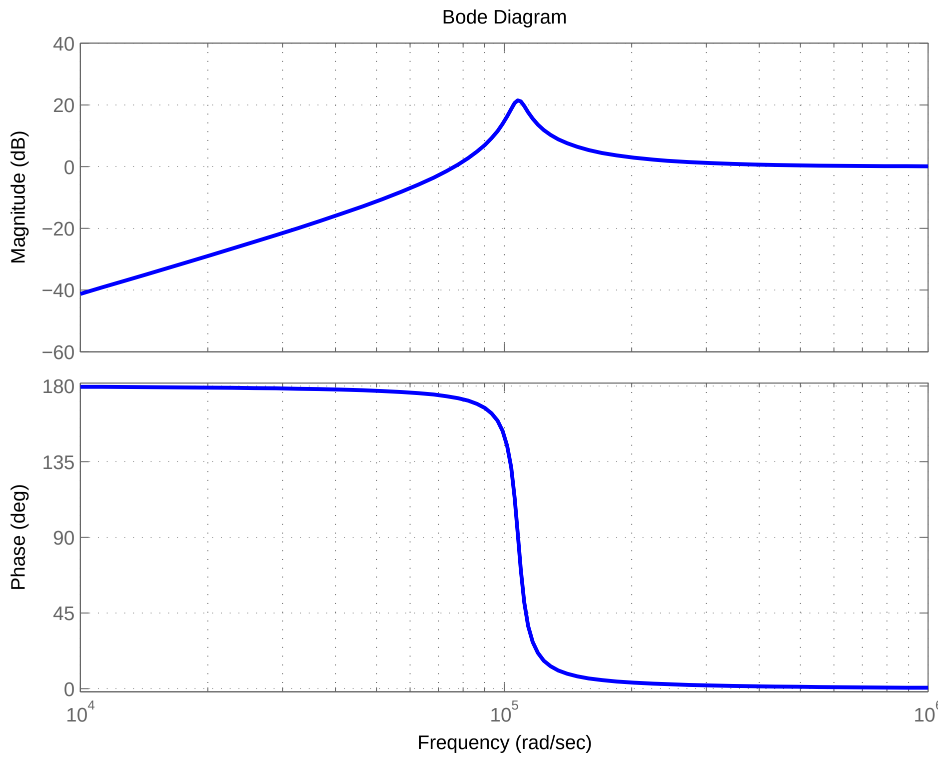


Figure 1.3: Transfer function $H_L(\omega)$ of the LCR series resonant circuit with a resonant angular frequency $\omega_L \simeq 10.7\text{krad/s}$.

1.2.3 Frequency Response with the Resistor Voltage Difference as Circuit Output

Considering the voltage difference across the resistor as the circuit output, we will have instead

$$H_R(\omega) = \frac{j\omega RC}{1 - \omega^2 LC + j\omega RC}.$$

Using the definition of Q and ω_0, and after some algebra, $H_R(\omega)$ becomes

$$H_R(\omega) = \frac{j\omega\frac{\omega_0}{Q}}{\omega_0^2 - \omega^2 + j\omega\frac{\omega_0}{Q}}. \tag{1.3}$$

Computing the magnitude and phase of $H_R(\omega)$, we obtain

$$
\begin{aligned}
|H_R(\omega)| &= \frac{\frac{\omega_0}{Q}\omega}{\sqrt{\left(\omega_0^2-\omega^2\right)^2+\left(\omega\frac{\omega_0}{Q}\right)^2}} \\
\arg\left[H_R(\omega)\right] &= \arctan\left(Q\,\frac{\omega_0^2-\omega^2}{\omega\omega_0}\right)
\end{aligned}
$$

The magnitude has maximum for

$$\omega_R^2 = \omega_0^2,$$

and the maximum is

$$|H_R(\omega_R)| = 1\,.$$

Far from the resonance ω_R, the approximate behavior of $|H_R(\omega)|$ is

$$
\begin{aligned}
\omega \ll \omega_R \quad &\Rightarrow \quad |H_R(\omega)| \simeq \frac{1}{Q}\,\frac{\omega}{\omega_0} \\
\omega \gg \omega_R \quad &\Rightarrow \quad |H_R(\omega)| \simeq \frac{\omega_0}{\omega}
\end{aligned}
$$

Figure 1.4 shows the magnitude and phase of $H_R(\omega)$. In this case the circuit is a first order band pass filter.

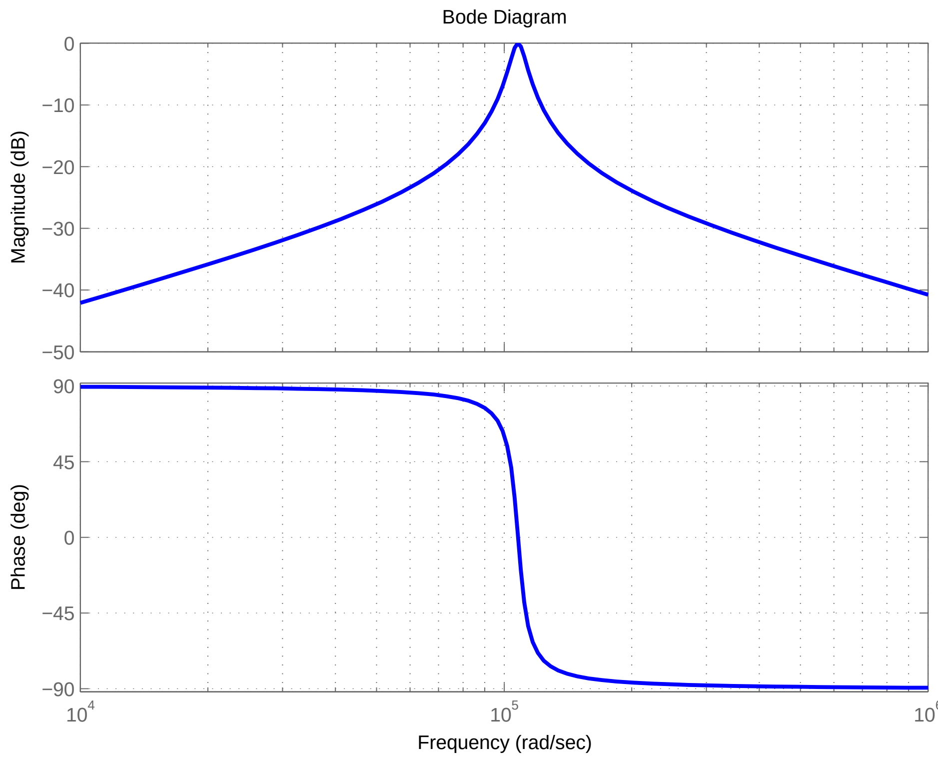


Figure 1.4: Transfer function $H_R(\omega)$ of the LCR series resonant circuit with resonant angular frequency $\omega_R \simeq 10.7$krad/s.

1.2.4 Transient Response

The equation that describes the LCR series circuit response in the time domain is

$$v_i = Ri + L\frac{di}{dt} + \frac{1}{C}\int_0^t i(t')dt' \,, \tag{1.4}$$

where $i(t)$ is the current flowing through the circuit and $v_i(t)$ is the input voltage.

Supposing that

$$v_i(t) = \begin{cases} v_0, & t > 0 \\ 0, & t \leq 0 \end{cases} ,$$

and differentiating both side of eq. 1.4, we obtain the linear differential equation

$$R\,\frac{di}{dt} + L\,\frac{d^2i}{dt^2} + \frac{1}{C}\,i = 0, \qquad t > 0$$

or, considering the definition of ω_0, and Q,

$$\frac{d^2i}{dt^2} + \frac{\omega_0}{Q}\,\frac{di}{dt} + \omega_0^2\,i = 0.$$

The solutions of the characteristic polynomial equation associated with the differential equation are

$$\lambda_{1,2} = -\frac{1}{2}\frac{\omega_0}{Q} \pm \omega_0\sqrt{\frac{1}{2Q^2} - 1}.$$

As usual, we will have three different solutions depending on the discriminant value

$$\Delta = \frac{1}{2Q^2} - 1\,.$$

Under-damped Case: discriminant less than zero $(Q > 1/\sqrt{2})$

In this case we have two complex conjugate roots and the differential equation solution is the typical exponential ring down

$$i(t) = i_0 e^{-\frac{\omega_0}{2Q}t}\sin\left(\omega_C t + \varphi_0\right), \qquad \omega_C^2 = \omega_0\left(1 - \frac{1}{2Q^2}\right)\,.$$

Critically Damped Case: Discriminant equal to zero$(Q = 1/\sqrt{2})$

In this case we have a critically damped current and no oscillation

$$i(t) = i_0 e^{-\frac{\omega_0}{2Q}t}$$

Over-damped Case: Discriminant greater than zero $(Q < 1/\sqrt{2})$

This is the case of two coincident solutions . We will have indeed, an exponential decay (no oscillations)

$$i(t) = i_0 e^{-\frac{\omega_0}{2Q}t}\left(Ae^{-\omega_C t} + Be^{+\omega_C t}\right), \qquad \omega_C^2 = \omega_0^2\left(1 - \frac{1}{2Q^2}\right),$$

Voltages across each single element can be easily computed considering the relation between $v(t)$ and $i(t)$.

Let's just write the voltage across the capacitor for the under-damped case. Considering that the integration operation in this case changes just the phase and creates an offset, the voltage across the capacitor, neglecting this offset, will be

$$v_C(t) = v_0 e^{-\frac{\omega_0}{2Q}t}\sin\left(\omega_C t + \psi\right).$$

1.3 The Tank Circuit or LCR Parallel Circuit.

Figure 1.5 shows the so called *LCR parallel resonant circuit* or *tank circuit*, where the source depicted with an arrow inside a circle is an ideal current source. The resistor of resistance r accounts for inductor resistance. Let's study the frequency and the transient response using the Thévenin representation shown in figure 1.6.

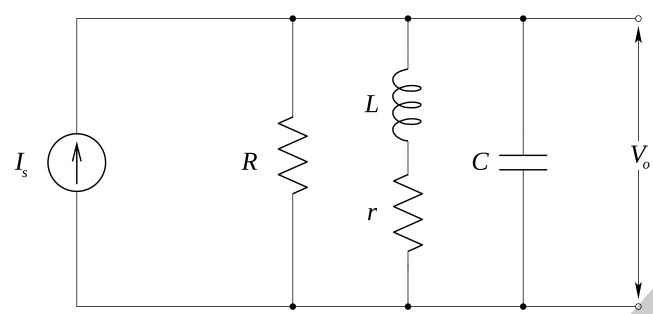


Figure 1.5: The tank circuit.

1.3.1 LCR Circuit Frequency Response

Using Thévenin theorem for the current source and R, the LCR parallel circuit considering the equivalent circuit as shown in figure 1.6 where the

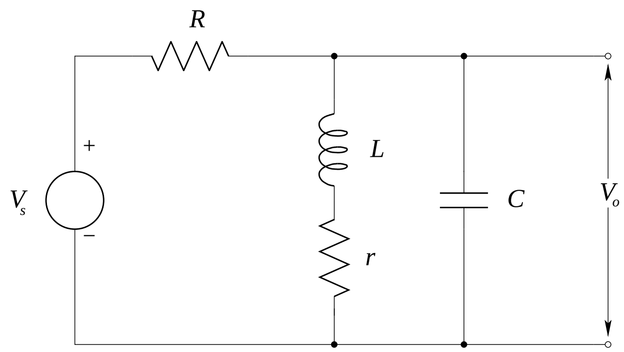


Figure 1.6: The tank circuit with the current source and the resistance R replaced with the Thévenin equivalent circuit.

current source and the resistor R have been replaced with the Thévenin circuit.

Considering that the current I of the current source can be written as

$$\begin{aligned} I &= \frac{V_i}{R}, \\ I &= Y\,V_o = \left(\frac{1}{R} + \frac{1}{r + j\omega L} + j\omega C\right) V_o, \end{aligned}$$

we have

$$\frac{V_i}{R} = \left(\frac{1}{R} + \frac{1}{r + j\omega L} + j\omega C\right) V_o \tag{1.5}$$

Defining the following complex quantity as

$$\frac{1}{r^*(\omega)} + \frac{1}{j\omega L^*(\omega)} = \frac{1}{r + j\omega L}, \tag{1.6}$$

and

$$R^* = R \,||\, r^*,$$

eq. 1.5 becomes

$$\frac{V_i}{R} = \left(\frac{1}{R^*} + \frac{1}{j\omega L^*} + j\omega C\right) V_o$$

After some algebra, we will have

$$\frac{V_o}{V_i} = \frac{j\omega L^*}{R^* - \omega^2 C L^* R^* + j\omega L^*} \frac{R^*}{R}. \tag{1.7}$$

Generalizing the definition of ω_0, and Q

$$\omega_0^* = \frac{1}{\sqrt{L^*(\omega)C}}, \qquad Q^* = R^*(\omega)\sqrt{\frac{C}{L^*(\omega)}},$$

and substituting in eq. 1.7 we finally obtain

$$H(\omega) = \frac{j\omega\omega_0^*/Q^*}{(\omega_0^*)^2 - \omega^2 + j\omega\omega_0^*/Q^*}\frac{R^*}{R}$$

Let's find the implicitly defined functions r^*, L^*. Using the term containing the inductance L in eq. 1.6, we obtain

$$\frac{1}{r + j\omega L} = \frac{1}{r\left[1 + \left(\frac{\omega L}{r}\right)^2\right]} + \frac{1}{j\omega L\left[1 + \left(\frac{r}{\omega L}\right)^2\right]}.$$

and finally

$$r^*(\omega) = r\left[1 + \left(\frac{\omega L}{r}\right)^2\right], \qquad L^*(\omega) = L\left[1 + \left(\frac{r}{\omega L}\right)^2\right]$$

1.3.2 Transfer Function

From the solution of the LCR parallel circuit we have

$$\begin{aligned} |H(\omega)| &= \frac{\frac{\omega\omega_0^*}{Q^*}}{\sqrt{\left[\left(\omega_0^*\right)^2 - \omega^2\right]^2 + \left(\frac{\omega\omega_0^*}{Q^*}\right)^2}}\frac{|R^*|}{R} \\ \arg(H(\omega)) &= \arctan\left\{Q^*\frac{\omega_0^2 - \omega^2}{\omega\omega_0}\right\}, \end{aligned}$$

whose bode plots are shown in figure 1.7.

1.3.3 Simplest Case

It is worthwhile to notice that if $r = 0$ we will have much simpler expressions, i.e.

$$\omega_0 = \frac{1}{\sqrt{LC}}, \qquad Q = R\sqrt{\frac{C}{L}}.$$

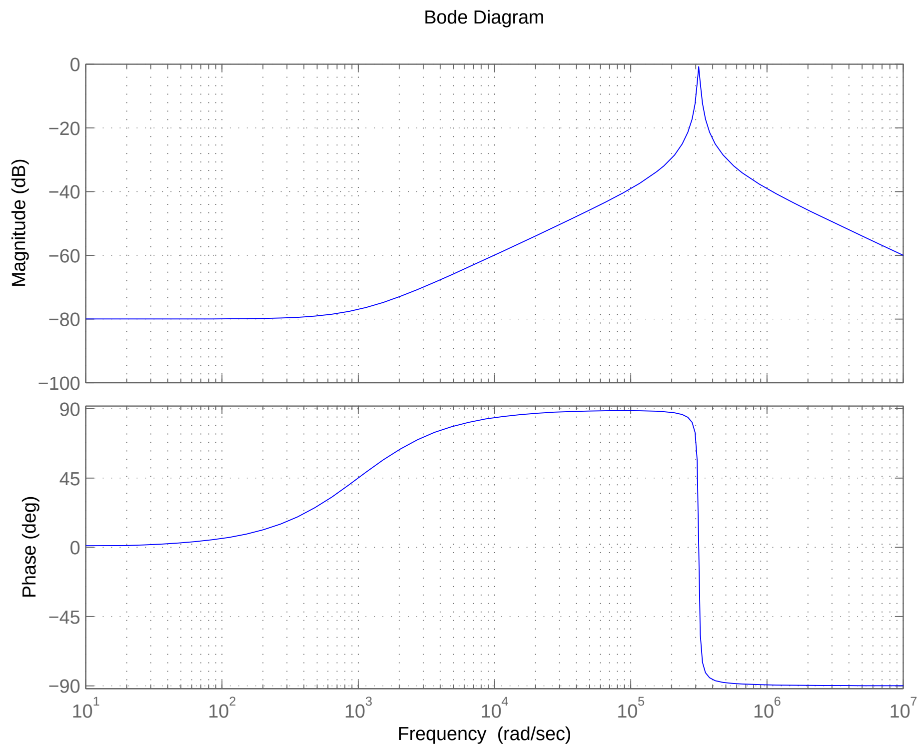


Figure 1.7: Typical bode plot of a LCR parallel circuit with resonant angular frequency near the acoustic band. As expected , if r is not zero, then the magnitude doesn't go to zero for $\omega = 0$.

and

$$H(\omega) = \frac{j\omega\omega_0/Q}{\omega_0^2 - \omega^2 + j\omega\omega_0/Q}$$

The magnitude and the phase will be

$$\begin{aligned} |H(\omega)| &= \frac{\frac{\omega\omega_0}{Q}}{\sqrt{\left(\omega_0^2 - \omega^2\right)^2 + \left(\frac{\omega\omega_0}{Q}\right)^2}} \\ \arg(H(\omega)) &= \arctan\left\{Q\frac{\omega_0^2 - \omega^2}{\omega\omega_0}\right\}, \end{aligned}$$

1.3.4 High Frequency Approximation

For high frequency $\omega \gg r/L$, we have

$$r^*(\omega) \simeq r\left(\omega\frac{L}{r}\right)^2, \qquad \Rightarrow \qquad L^* \simeq L$$

and ω_0 becomes

$$\omega_0 \simeq \frac{1}{\sqrt{LC}}.$$

Evaluating the several defined quantities at ω_0, we will have

$$\begin{aligned} r^*(\omega_0) &\simeq \frac{L}{rC}, \\ R^*(\omega_0) &\simeq \frac{LR}{RCr+L} \\ Q^*(\omega_0) &\simeq \frac{LR}{RCr+L}\sqrt{\frac{C}{L}} \end{aligned}$$

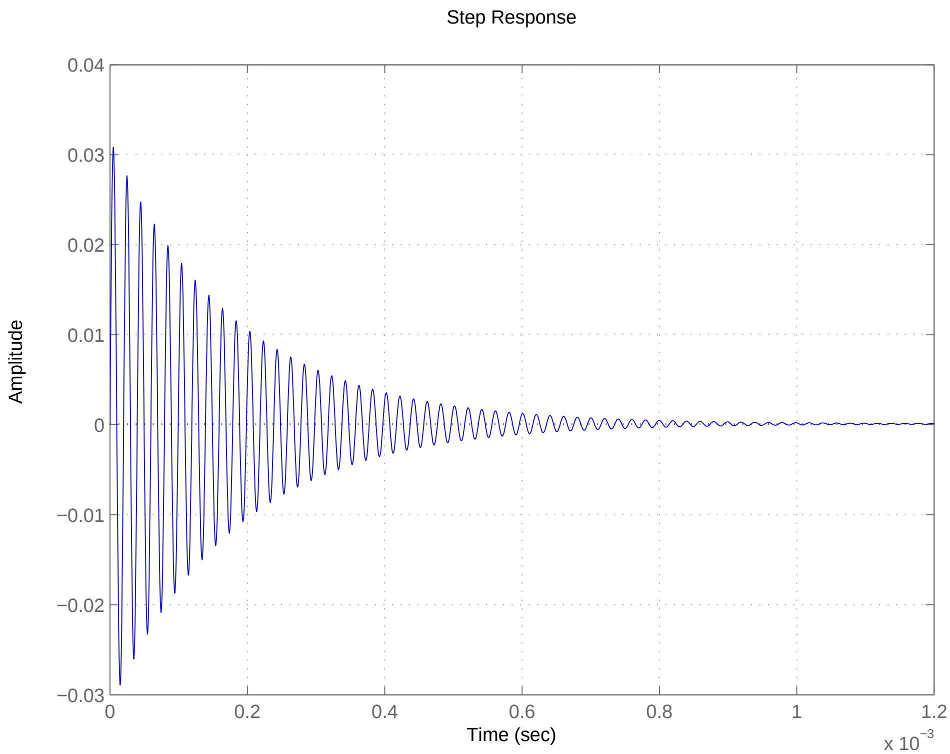


Figure 1.8: Typical step response of a LCR parallel circuit near the acoustic band.

1.3.5 LCR Parallel Circuit Transient Response

Let's briefly analyze the response to a step of the LCR parallel circuit for the under-damped case.

If we define the following quantity

$$\gamma = \frac{1}{2Q},$$

called damping coefficient, and if $0 < \gamma < 1$, then we will have at the circuit output

$$v(t) = v_0 \frac{2\gamma}{\gamma - 1} e^{-\omega_0 \gamma t} \cos\left(\sqrt{1-\gamma^2}\,\omega_0 t + \varphi_0\right) + v_1 \,.$$

The voltage output $v(t)$ is a damped sinusoid with angular frequency $\sqrt{1-\gamma^2}\,\omega_0$ and time constant $\tau = 1/\omega_0\gamma$. The DC offset v_1 depends on the inductor resistance r and the initial step.

Figure 1.8, a typical step response of the LCR circuit shows a ring-down with a DC offset.

1.4 Laboratory Experiment

Real inductors have not negligible resistance. To build a LCR series circuit with a highest quality factor it is indeed necessary to minimize the resistance of the circuit by mounting in series the inductor and the capacitor only. Typical effective resistance of the inductors used in the laboratory is about 10Ω to 80Ω at resonance .

Because of the internal resistance of the function generator (the best scenario gives $\sim 50\Omega$) is then comparable at some frequencies to LCR load, we will expect that the approximation of ideal generator will be no longer valid.

Moreover, harmonic distortion of the function generator will be quite evident in the LCR series circuit because of the dependence of the load on the frequency.

An estimation of a ring-down time constant τ can be obtained as follows. From the ring-down equation we have that after a time $t = \tau$ the envelope maximum amplitude is reduced by a factor $1/3$ ($e \simeq 1/2.718$). This means that we can easily estimate τ by just measuring the time needed to reduce the amplitude down to about $1/3$ of its initial value. Another but quite coarse way is to count how many periods n^* the amplitude takes to decrease to $1/3$ of its initial value. Then the estimation will be

$$\tau \simeq T n^* = \frac{n^*}{\nu_{res}} ,$$

where T, and ν_{res} are respectively the period and the frequency of the oscillation. Considering that $Q = \pi \nu_{res} \tau$ then

$$Q \simeq \pi n^* .$$

The quality factor can also be estimated from the frequency response considering that

$$Q = \frac{\nu_{res}}{\Delta\nu} ,$$

where $\Delta\nu$ is the Full Width at Half Maximum (FWHM) of the peak resonance.

1.4.1 Pre-laboratory Exercises

It is suggested to read the appendix about the electromagentic noise to complete the pre-lab problems and the laboratory procedure.

1. Determine the capacitance C of a LCR series circuit necessary to have a resonant frequency $\nu_C = 20\text{kHz}$ if $L = 10\text{mH}$, and $R = 10\Omega$. Then, calculate Q, τ, ν_0, $(\omega = 2\pi\nu)$ of the circuit.

2. Find the LCR series input impedance Z_i and plot its magnitude in a logarithmic scale. Determine at what frequency is the minimum of $|Z_i|$.

3. Supposing that the internal resistance of the function generator is $R_s = 50\Omega$, and using the previous values for L, C, and R, calculate the circuit input voltage attenuation at the frequency of $|Z_i|$ minimum and at twice that frequency.

4. Determine the capacitance C of a tank circuit necessary to have a resonant frequency $\nu_C = 20$ kHz if $L = 10\text{mH}$, $R = 10\text{k}\Omega$, and $r = 10\Omega$. Use the high frequency approximation. Then, calculate Q, τ, ν_0, of the circuit.

5. Estimate the time constant τ of the ring-down in figure 1.8. Supposing that $R = 10\text{k}\Omega$, estimate r from figure 1.7.

6. Calculate the maximum frequency of the EM field isolated by a Faraday cage with a dimension $d = 10\text{mm}$ (hint: consult the proper appendix).

1.4.2 Procedure

1. Build a LCR series circuit with a resonant frequency of around 20kHz, using inductance, capacitance, and resistance values calculated in the pre-lab problems. Then, do the following steps:

   (a) Using the oscilloscope and knowing the expected magnitude and phase values at the resonant frequency ν_C, find ν_C and compare it with the theoretical value computed using the components measured values.

   (b) Verify the circuit transfer function $H_C(\nu)$ using the data acquisition system and the proper software.

   (c) Estimate the quality factor Q of the circuit from the transfer function measurement and compare it with the theoretical value.

(d) Explain why the input voltage V_i changes in amplitude if we change frequency.

(e) Considering the harmonic distortion of the function generator, explain why the frequency spectrum of the input signal changes quite drastically when we approach the resonance ν_C.

(f) Download the simulation file from the ph5/105 website for the LCR series circuit, input the proper components values, run the AC response simulation, and find the discrepancies beteween your measurement and the simulation.

(g) Modify the simulated circuit to qualitatively account for the eventual notch measured between 100 kHz and 1 MHz (hint: use the inductor model specified in the appendix considering the extra capacitor only).

2. Build a LCR parallel circuit with a resonant frequency around 20kHz, using inductance, capacitance, and resistance values calculated in the pre-lab problems. Then, do the following steps:

(a) Using the oscilloscope and knowing the expected magnitude and phase values at the resonant frequency ν_C, find ν_C and compare it with the theoretical value computed using the components measured values.

(b) Verify the circuit transfer function $H_C(\nu)$ using the data acquisition system and the proper software.

(c) Estimate the quality factor Q of the circuit from the step response.

(d) Download the simulation file from the ph5/105 website for the LCR parallel circuit, input the proper components values, run the AC response simulation, and find the discrepancies beteween your measurement and the simulation.

(e) Modify the simulated circuit to qualitatively account for the eventual notch measured between 100 kHz and 1MHz (hint: use the capacitor model specified in the appendix considering the extra inductors only).

3. Check the effect of the Faraday cage (a metallic coffee can) using 10x probe connected to the oscilloscope. Add a 1m long wire to increase the antenna effect.
   Note the differences when the antenna is approached to the fluorescent lights, and when you touch the antenna.
   Keeping the cage in the same position and without touching the cage, explain what you observe and coarsely estimate the amplitude and frequency content of the picked-up signal in the following conditions:

   (a) Antenna outside the cage,

   (b) Antenna inside the cage,

   (c) Antenna inside the cage with ground probe connected to the cage.

Chapter 2

Diodes and Transistors

2.1 Introduction

In this chapter we will analyze two new electronic devices, the semiconductor diode and the bipolar junction transistor (BJT). For a better understanding of their behavior and characteristics, we will also introduce some basic applications.

Unfortunately, there will be no time to study the quite complex physics of semiconductors, and especially the conduction mechanism, which substantially differs from that of metals. The interested student should look for a course and books on solid state physics.

It is important to notice that to quickly grab how the BJT device works, it is fundamental to acquire a clear understanding of the semiconductor diode's behavior.

2.2 The Semiconductor Junction (Diode)

The *semiconductor junction* or *semiconductor diode* is a device which shows non-linear behavior due to its peculiar conduction mechanism.

In fact, if I_D and V_D are the current and the voltage difference across the junction, we will have

$$I_D(V_D) = I_0(e^{\frac{-qV_D}{\eta k_B T}} - 1), \tag{2.1}$$

where I_0 is the reverse saturation current, $k_B = 1.3807 \cdot 10^{-23}$J/K, the

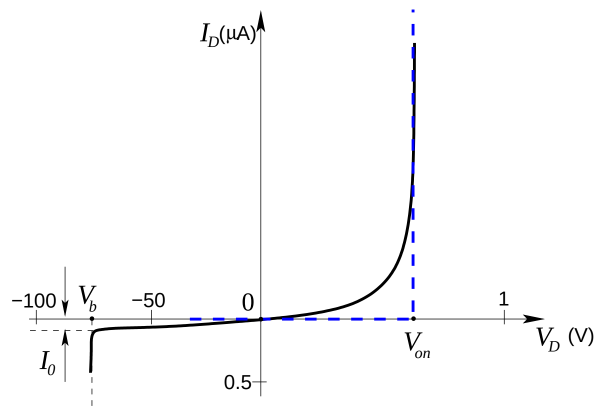


Figure 2.1: Diode characteristic (continuous curve), simplified diode characteristic (dashed curve). Note the different scales in first and third quadrant of the diode characteristic plot.

Boltzmann constant, T the absolute temperature , $q = -1.60219 \cdot 10^{-19}$C, the electron charge, and η a dimensionless parameter which depends on the diode type. Considering that the ambient temperature is $T \simeq 300$K, we will have $k_B T \simeq 4.14 \cdot 10^{-21} J \simeq 0.026 eV$. For silicon diodes the reverse saturation current I_0 is of the order of few tenths of nano-amperes.

Instead of following Ohm's law, the semiconductor junction follows an exponential law. Deviations from this law are negligible depending on the current magnitude and the diode characteristics.

Figure 2.1 shows standard symbols for a semiconductor diode and the I-V characteristic. The break-down voltage V_b reported in the same figure is the reverse voltage which essentially short circuits the junction (typically between -100V and -50V). This behavior is not accounted in equation (2.1), and is generated by the so called avalanche multiplication mechanism and the Zener mechanism[1].

[1] The thermally generated carriers accelerated by the electric field have enough energy to disrupt the electrons bond of the crystal atoms producing new carriers (electron-holes pairs). The new and accelerated pairs generate new carriers producing an avalanche of carriers, and indeed a break-down current.

A sufficient strong electric field can also disrupt electrons bonds creating an electron-hole reverse current. This effect is called Zener Breakdown mechanism.

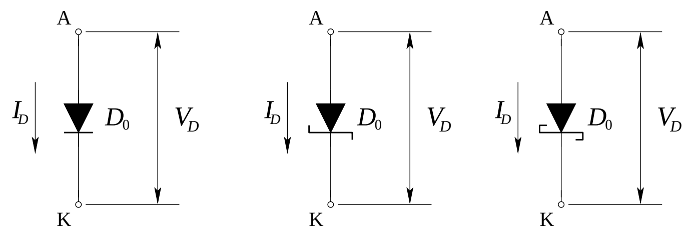


Figure 2.2: diode standard symbols. Starting from left, diode symbol , Zener diode symbol, and Schottky diode symbol. Diode terminals A, and K are respectively called anode and cathode.

A simplified model of the junction diode is that of a perfect switch, i.e.

$$I_D(V) = \begin{cases} \infty & V \geq V_{on} \\ 0 & V < V_{on} \end{cases},$$

where V_{on} is the diode *turn-on voltage* or *cut-in voltage*, which depends on the junction type and on the current magnitude. For current up to $I_D \sim 100$ mA, silicon diodes have $V_{on} \simeq 0.6$V, and germanium diodes have $V_{on} \simeq 0.3$V .

For voltages greater than V_{on}, the diode is a short circuit (current is not limited by the diode) and is said to be *forward biased*. For smaller values it is an open circuit (current across the diode is zero) and is *reverse biased*.

2.2.1 Zener Diodes

Zener diodes are particular semiconductor diodes with adequate power dissipation to operate in the break-down voltage region. They have a well defined V_b, with values ranging from about few volts to several hundreds volts. Zener diode symbol is shown in Figure 2.9. Approximating the characteristics with a piecewise linear relationship, we have

$$I_D(V) = \begin{cases} -\infty & V < V_b \\ 0 & 0 \leq V < V_{on} \\ +\infty & V \geq V_{on} \end{cases},$$

Often, the break-down curve is virtually vertical so that the previous approximation of the reverse biased region is quite good.

2.2.2 Schottky Diodes

A junction made of a semiconductor and a metal can behave like a semiconductor diode[2]. For example, Lightly doped silicon and aluminum can form a semiconductor junction. Such kind of devices, called *Schottky barrier diodes* (or simply *Schottky diodes*), still follow the diodes characteristics (2.1) with usually a lower turn-on voltage V_{on} and a larger in magnitude reverse saturation current I_s. The symbol for Schottky diode device is shown in Figure 2.9.

2.3 Diode Dynamic Impedance

For linear devices the current is proportional to the applied voltage and for a given frequency the impedance (V/I) is constant. With non-linear circuits this is not true anymore, but we can generalize the impedance concept introducing the dynamic impedance

$$R_d = \frac{dV}{dI}$$

Let's apply this definition to the diode. Starting from the I-V characteristic equation and neglecting the reverse saturation current, after some algebra we obtain

$$V_D = \eta \frac{k_B T}{q} \ln \frac{I_D}{I_0} .$$

Taking the derivative on both sides we obtain

$$R_d = \eta \frac{k_B T}{q} \frac{1}{I_D}$$

As we can see, the dynamic impedance of the diode depends on the current I_D.

Considering a silicon diode with a typical value of $\eta = 2$, we will have

$$R_d(I_D) \simeq \frac{5.2 \cdot 10^{-4}}{I_D}, \qquad I_D = 1\text{mA} \quad \Rightarrow R_d \simeq 0.52\Omega .$$

For small variations of the current around 1mA, we can assume that the impedance of a forward biased diode with $\eta = 2$ is $\sim 0.5\Omega$. The dynamic impedance concept will be quite useful for studying the bipolar junction transistor.

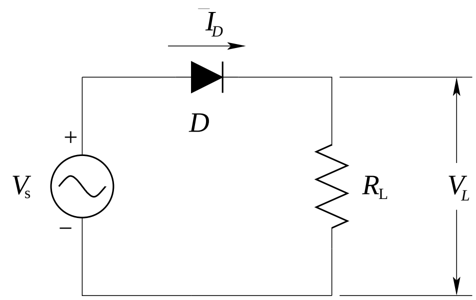


Figure 2.3: Half-wave rectifier circuit.

2.4 Practical Circuits

To better understand the behavior of a semiconductor junction, let's analyze a few typical applications of semiconductor diodes. Some other applications in connection to other components will be studied in the following chapters.

2.4.1 Rectifiers, AC to DC Conversion

The purpose of a rectifier circuit is to convert alternating current into a unidirectional current. This can be achieved using semiconductor diodes. The typical alternating current to direct current converter is a rectifier connected to an active low pass filter with a so called regulator circuit, which smooths the rectifier output and minimizes ripples. The simplest regulator is a capacitor placed in parallel with the rectifier output. Regulators can be easily found in literature (see [1]).

2.4.1.1 Half-Wave Rectifier

The simplest rectifier circuit is the so called half-wave rectifier shown in Figure 2.3.

Using the diode ideal characteristic, it is quite straightforward to predict the voltage difference across the the resistor R_L. In fact, when the sinusoidal signal is positive, it will forward bias the diode and we will have a voltage drop across the resistor $V_L = RI$. For the negative half cycle, because the diode is reverse biased V_L must be zero.

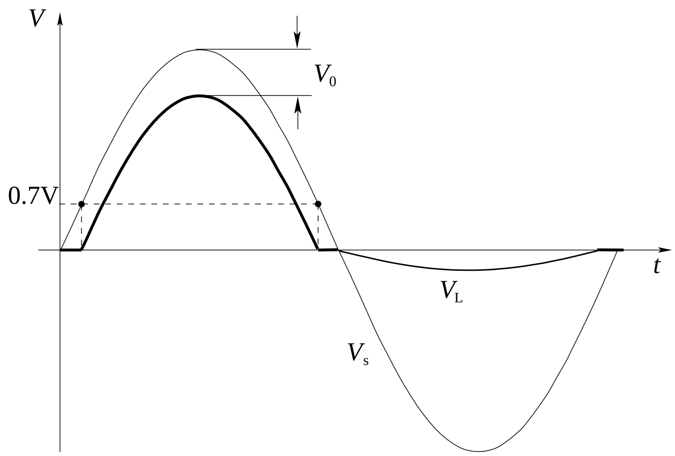


Figure 2.4: Voltage difference across the load connected to the half-wave rectifier output.

Considering the diode threshold voltage V_0, and the diode resistance R_f during the positive half cycle we will have

$$V_L = \frac{R_L}{R_f + R_L}(V_s - V_0),$$

and if

$$R_L \gg R_f \quad \Rightarrow \quad V_L \simeq (V_s - V_0).$$

During the negative half cycle we will have

$$V_L = \frac{R_L}{R_r + R_L} V_s,$$

and if

$$R_L \ll R_r \quad \Rightarrow \quad V_L \simeq \frac{R_L}{R_r} V_s \simeq 0.$$

The main disadvantage of this circuit is the very poor efficiency (less than 50% of current is rectified). In fact, instead of rectifying the entire signal the circuit chops the negative half cycle out (see Figure 2.4).

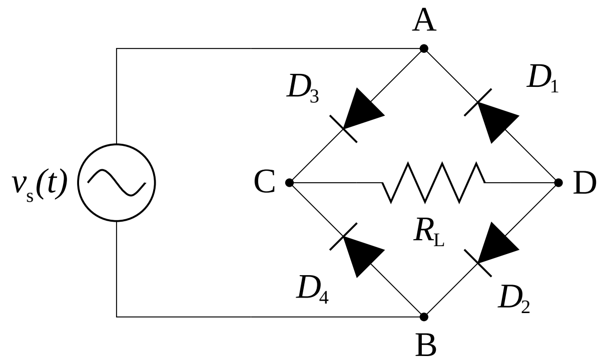


Figure 2.5: Full-wave rectifier bridge circuit or simply bridge rectifier.

2.4.1.2 Full-Wave Rectifier Bridge

The Full-Wave rectifier bridge (see Figure 2.5), a more efficient way of rectifying an AC current, uses four arranged diodes in the so called bridge configuration. To understand the circuit "logic", let's consider the two possible states of the nodes A and B shown in Figure 2.5.

- When the node A is positive (B negative) the diodes D_2, and D_3 are forward biased (i.e. the diodes are a "short circuit") and D_1, and $D_4$are reverse biased (i.e. the diodes are an "open circuit"). The current flows through the resistor R_L and the node C is positive.

- When the node A is negative (B positive), the diodes D_1, and D_4 are forward biased (short circuit) and D_2, and D_3 are reverse biased. The current flows through the resistor R_L and the node C is still positive.

Using the full-wave rectifier we will indeed have the negative half cycle rectified as shown in Figure2.6.

2.4.2 Voltage Limiter (Diode Clamp)

Diodes can be used to limit the voltage applied to an input as shown in Figure 2.7. Let's consider the diode D_1connected to V_{max}. If V_i exceeds $V_{max} + V_{on}$ the diode is not reverse biased anymore and starts conducting, i.e the circuit limits the input voltage V_i to $V_{max} + V_{on}$. Analogously, D_2 limits the minimum input voltage V_i to $V_{min} + V_o$. The resistor is necessary to limit the current flowing through the diodes. In fact, without the resistor

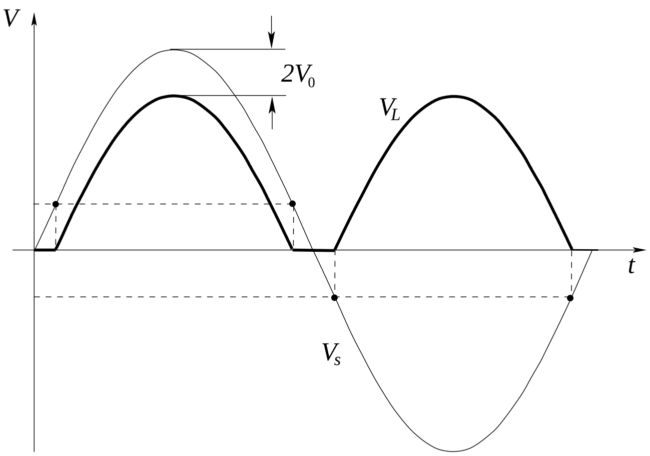


Figure 2.6: Voltage difference across the load connected to the full-wave rectifier output

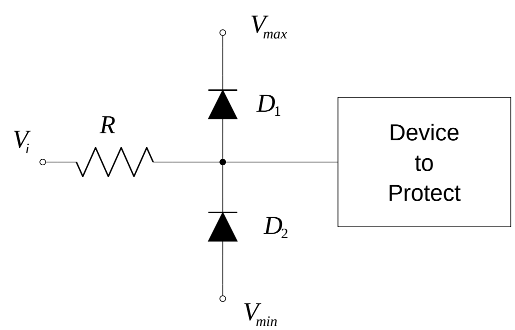


Figure 2.7: Diode clamps circuit.

if we exceed one of the voltage limits an excessive current can destroy the forward biased diode junction. The worst scenario is when the broken diode becomes an open circuit and then the device to protect becomes completely unprotected.

2.5 The Bipolar Junction Transistor (BJT)

The *bipolar junction transistor* is essentially a device formed by two semiconductor junctions which share one semiconductor layer (see Figure 2.8).

The common layer is called the *base* and the two others are the *collector*

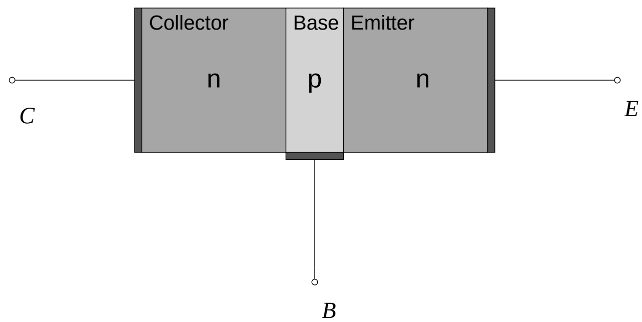


Figure 2.8: Qualitative physical model of a npn junction.

and *emitter*. We will have then the *emitter-base* and the *collector-base* junctions.

There are two types of BJT: the *npn* and the *pnp transistor*. In the pnp transistor the collector and the emitter are p-type and the base is n-type. The npn transistor has a p-type base , and n-type collector and emitter. Standard symbols for both types are shown in Figure 2.9.

Because the two junctions have two possible states (forward or reverse biased), the BJT can have four possible operating modes as shown in the following table

Operating Mode	Bias Emitter-Base	Bias Collector-Base
Forward-Active	Forward	Reverse
Cutoff	Reverse	Reverse
Saturation	Forward	Forward
Reverse-Active	Reverse	Forward

Forward-Active:

The BJT approximates a current-controlled source of current as explained in section 2.5.2.

Cutoff:

Both junctions are reverse biased. Neglecting the reverse saturation current, no current flows through the junctions. This mode, together with the saturation mode, is used to implement the switch device (see section2.5.5).

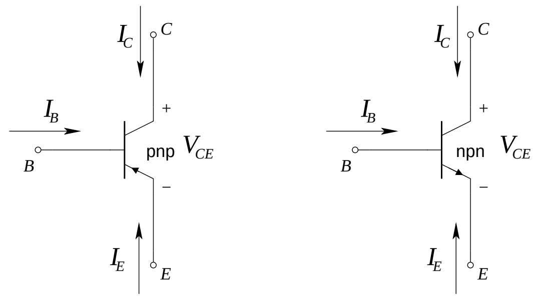


Figure 2.9: Standard circuit symbols for npn and pnp transistors.

Saturation:

Both junctions are forward biased, and the current I_C flows from the collector through the emitter.

Reverse-Active:

The BJT still approximates a current-controlled source of current, but the amplification factor is usually less than that of the forward-active mode.

2.5.1 The Collector Emitter Characteristic

Figure 2.10 shows collector emitter characteristic curves family of a typical npn transistor. Each curve corresponds to a given value of the base current I_B, with the base emitter junction forward biased.

The curves have three regions which are called, the *saturation*, *forward-active*, and *breakdown* regions. The break-down region starts for V_{CE} values larger than those shown in the plots .

Saturation Region

The saturation region is where the collector emitter voltage difference V_{CE} slightly changes as a function of the collector current I_C. For the 2N2222 this regions is where V_{CE} is between 0V to about 0.3V.

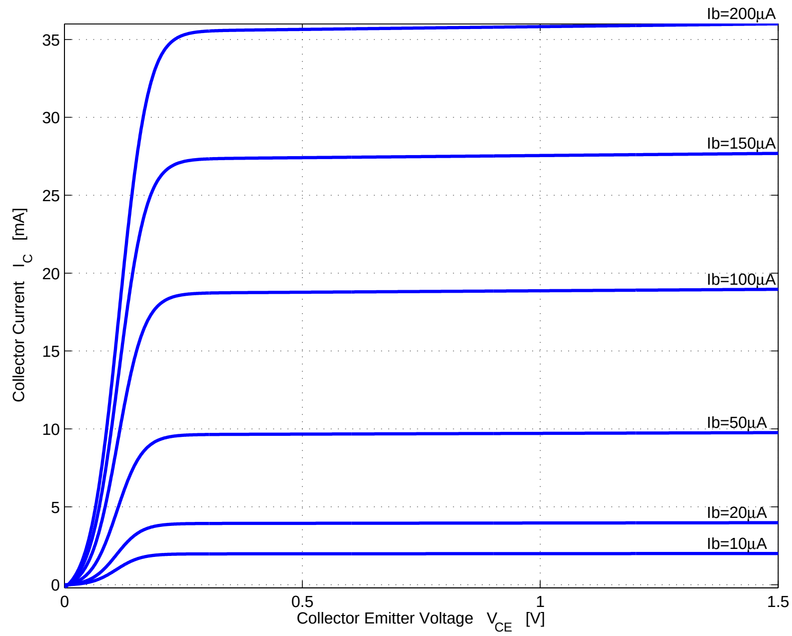


Figure 2.10: Collector Emitter voltage characteristics for the 2N2222 npn transistor. The value above each curve is the corresponding base current I_B.

Forward-Active Region

The collector current I_C slightly changes as a function of the collector emitter voltage V_{CE}. Normally, this region is quite larger than the saturation region. For the 2N2222 it is where V_{CE} is between 0.3V to about 50V.

Break-Down Region

This is the region where the V_{CE} doesn't change and I_C rapidly increases. In this case, the conduction in the junction is produced by the avalanche mechanism. For the 2N2222 this region starts from $V_{CE} > 60$V.

2.5.2 The BJT as a Current-Controlled Current Source (CCCS)

As stated before, the bipolar junction transistor is a device that approximates a current-controlled source of current CCCS (see Figure 2.11). In other words, because its current output i_o is proportional to the current

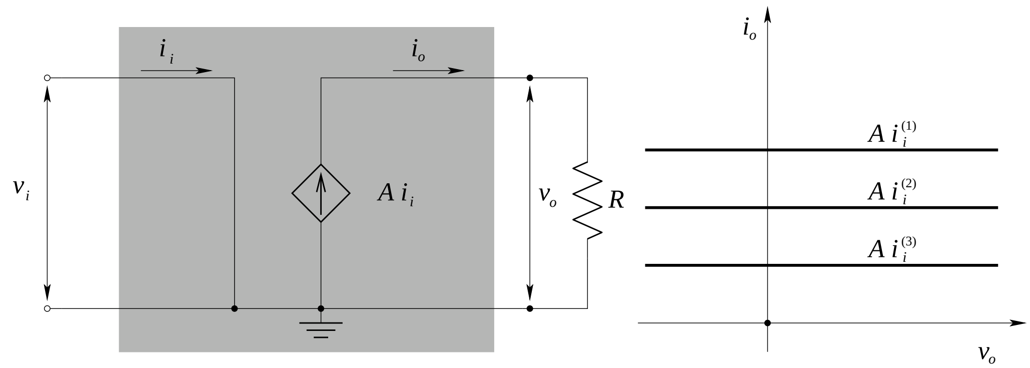


Figure 2.11: Ideal current controlled source (diamond symbol), i.e. the current output i_o is proportional to the current input i_i, and is independent of the load R. In other words, if we change the load R and v_o consequently, i_o stays constant.

input i_i we can linearly control i_o by changing i_i, i.e.

$$i_o(t) = \beta_F\, i_i(t).$$

if $|\beta_F| > 1$ then the BJT is a current amplifier.

As shown in Figure 2.11, once i_i is set i_o must be constant independently of the load R placed at the output. If the voltage across the output $v_o$changes we don't expect to see any changes on i_o. The curve height simply depends on the current input i_i.

This approximation is valid for the so called small signal model and the low frequency model. Non linearities arise for large signals and at high frequency the response cannot be flat.

It is clear from the V_{CE} characteristic that, if we want to use the BJT as CCCS , we have to bias it with a DC voltage to work in the forward-active region.

2.5.3 BJT Simplified DC Model

The simplified DC model of the BJT for the forward-active mode is shown in Figure 2.12 with two different arrangements. The first mimics the topology of the BJT symbol, and the second the topology of the CCCS in Figure 2.11. This model is good enough to properly bias the transistor to work as an amplifier.

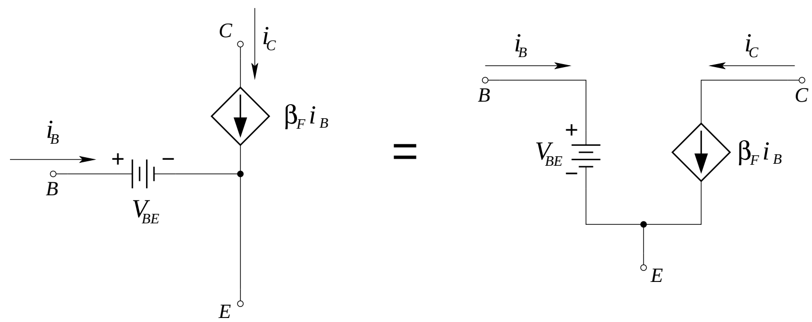


Figure 2.12: Simplified DC model for the bipolar junction transistor working in forward-active mode. The two drawings are just two different arrangement of the same circuit.

The current controlled current source represents the V_{CE} characteristic in the forward-active region. The battery in the base emitter circuit represents the voltage across the base-emitter forward biased junction (it could be replaced with a diode). A typical value is $V_{BE} = 0.7$V.

2.5.4 The BJT as an Amplifier

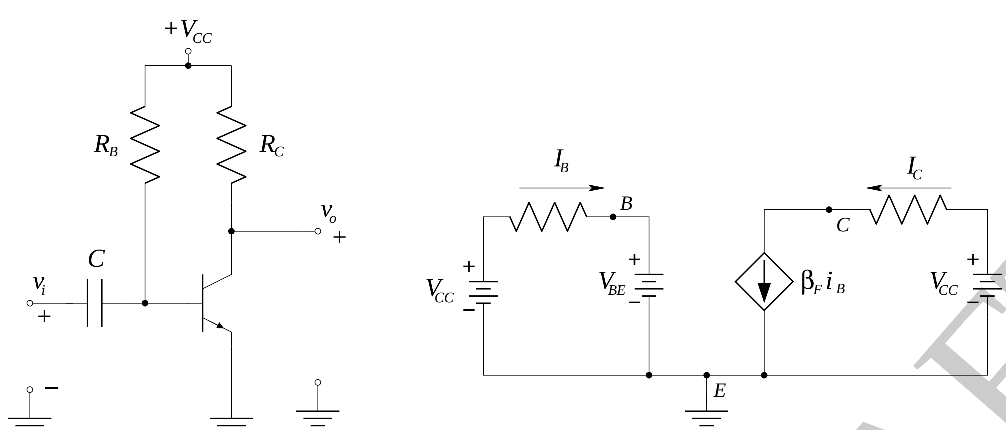


Figure 2.13: The BJT as an AC basic amplifier (left), and same circuit using the forward-active DC model (right).

Left circuit of Figure 2.13 shows the basic configuration of a BJT as a simple current amplifier. Resistors R_B and R_C are chosen to properly bias and limit the currents across the junctions. The capacitance at the input is necessary to prevent the DC bias from reaching the device connected to the amplifier input. Let's better analyze how to properly bias the transistor junctions.

2.5.4.1 BJT Amplifier Bias

To obtain the largest voltage dynamic range, and considering the V_{CE} characteristic, and neglecting the saturation region, we must have

$$V_{CC} \simeq 2\,V_{CE}\,. \tag{2.2}$$

Plugging the forward-active DC model into the amplifier circuit as shown in Figure 2.13, we will have[2]

$$V_{CC} = V_{CE} + R_C I_C,$$

Considering equation2.2 and the previous equation, the collector resistor value will be

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{V_{CE}}{\beta_F I_B}.$$

For the base resistor we will have

$$V_{CC} = V_{BE} + R_B I_B,$$

and finally

$$R_B = \frac{2V_{CE} - V_{BE}}{I_B}\,.$$

This circuit is not very useful because the junctions bias and the gain depend on β_F, which is quite often not well know and can easily vary by a factor of two for the same transistor. Moreover, $\beta_F$is quite sensitive to temperature fluctuations. Anyway, this circuit is pedagogically interesting because of it simplicity.

[2]The repeated index is a common convention used to distinguish between the voltage of the transistor's connections and the source voltages applied to the transistor connections. In this case between the collector voltage V_C and the source voltage V_{CC}.

Numerical Example

A typical BJT a transistor has V_{CE} between 1V and 10V. Considering the following parameters

$$\begin{cases} \beta_F &= 100 \\ V_{CE} &= 5\text{V} \\ V_{BE} &= 0.7\text{V} \\ I_B &= 80\mu\text{A} \end{cases} \Rightarrow \begin{cases} R_C &\simeq 625\Omega \\ R_B &\simeq 116.25\text{k}\Omega \\ V_{CC} &\simeq 10\text{V} \end{cases} .$$

2.5.4.2 BJT Amplifier Gain, Input and Output Impedance (Low Frequency Model)

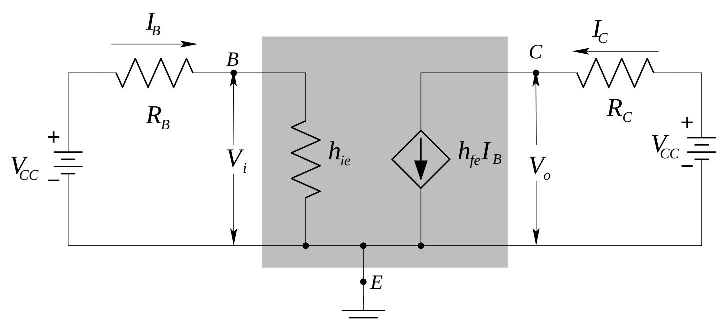


Figure 2.14: BJT basic amplifier using the low frequency model (gray box). The parameters $h_{fe} = \beta_F$and h_{ie} are provided by the manufacturer

Because the emitter-base junction is forward biased, the input impedance seen from the points B and E is quite low. This consideration with the fact that the BJT approximates a CCCS is sufficient enough to define a model for the BJT transistor response for the low frequency region. Figure 2.14 shows the model applied to the basic amplifier. The resistance h_{ie} is indeed the dynamic input impedance of the forward biased emitter-base junction.

From Figure 2.14 we can easily calculate the amplifier voltage gain, which is

$$|A_v| = \frac{R_C I_C}{h_{ie} I_B} = h_{fe}\frac{R_C}{h_{ie}} \qquad (\beta_F = h_{fe})$$

Considering that the ideal current source is an open circuit and the ideal voltage source is a short circuit, we will have

$$R_i \simeq R_B || h_{ie}, \qquad R_o \simeq R_C .$$

Thermal fluctuations can substantially change the response of the BJT. A way to avoid such kind of behavior is to add a feedback network. Essentially, a feedback network samples the output and sends it back to the input with negative sign minimizing the output fluctuations. For example, if the amplifier gain increases because of a temperature increase, the feedback signal will increase as well reducing the input signal by the amount necessary to keep the gain constant. Feedback networks can create instabilities due phase delays in the loop (the feedback signal can change sign). It is indeed necessary to satisfy stability criterion to avoid oscillations. A detailed explanation of feedback theory can be found in [2] and [3].

2.5.5 BJT as Switch

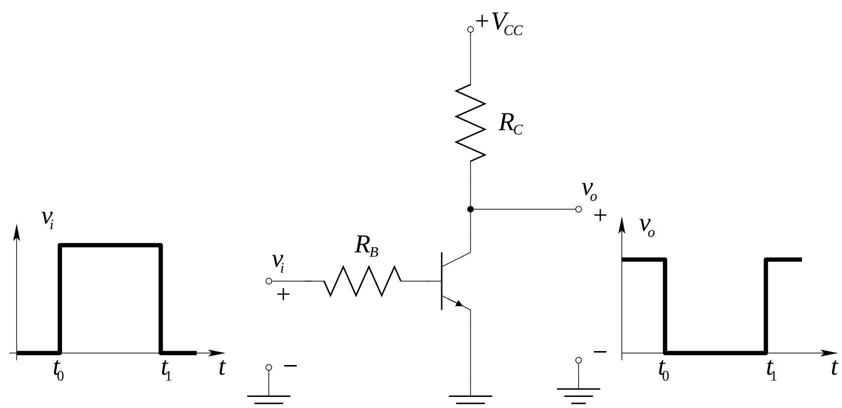


Figure 2.15: BJT as a switch

Figure 2.15 shows a npn BJT configured as a switch. In this case, the function of the two resistors R_B and R_C are just to limit the current flowing through the transistor junctions.

The input voltage v_i control the output state of the switch. For sake of simplicity let's neglect the reverse currents components to study the circuit.

- If $v_i = 0$, The emitter-base junction is reverse biased and no current flows through the circuit. This implies that $v_o \simeq V_{CC}$ and (BJT in cutoff state).

- If $v_i = V$ and supposing that this voltage forward bias both junctions we will have $v_o \simeq 0$ (BJT in saturation).

Let's consider now the BJT reverse currents.

- If $v_i = 0$, we will have $i_C = I_{CO}$ and $v_o = V_{CC} - I_{CO}R_C$. Because $I_{CO} \sim$ 1nA $I_{CO}R_C$ is negligible and $v_0 = V_{CC}$.
- If $v_i = V$, then v_0 is essentially the voltage drop $V_{BE}$of the forward biased base-emitter junction $v_o = 0.7$V.

2.5.6 BJT as Diode

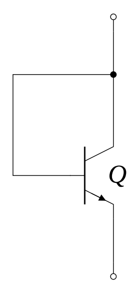


Figure 2.16: BJT as diode.

Figure 2.16 shows the typical configuration used to make a BJT working as simple diode. The emitter-base junction acts as a simple semiconductor diode. Short circuiting the collector-base ensures that the collector-base junction is always reverse biased.

2.5.7 Current Mirror

Let's consider the left circuit shown in Figure 2.17 where V_{CC}forward bias the emitter-base junction. From the KVL obtain

$$I_R = \frac{V_{CC} - V_{BE}}{R}.$$

If V_{CC} and R are kept constant ($V_{BE} = 0.7$, typically) then I_R is constant as well. Applying the KCL to node we obtain

$$I_R = I_C + I_B$$

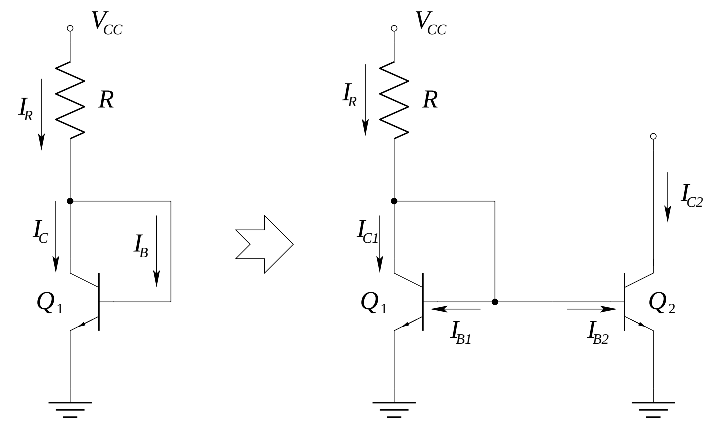


Figure 2.17: BJT as diode.

and considering that

$$I_c = \beta I_B$$

we will finally have

$$I_R = \left(1 + \frac{1}{\beta}\right) I_C. \quad \Rightarrow I_C \simeq I_R.$$

The collector current I_C is indeed constant if $V_{CC}$and R are kept constant.

Let's now consider the circuit on the right-hand side of Figure 2.17. Because of the KVL we will have

$$V_{BE1} = V_{BE2}$$

Supposing that the two transistors Q_1 and Q_2 are perfectly identical and because they have the same V_{BE}we must have

$$I_{C1} = I_{C2}.$$

We will have indeed that the output I_{C2} will work as a constant current source.

Let's analyze the stability of the circuit for a change on the transistor parameter β. From the KVL and KCL we have

$$\begin{aligned} I_R &= \frac{V_{CC} - V_{BE}}{R} \\ I_R &= I_C + 2I_B \end{aligned}$$

After some simple algebra and considering that $I_C = \beta I_B$we will have

$$I_C = \frac{\beta}{\beta + 2} \frac{V_{CC} - V_{BE}}{R}$$

Studying the fluctuation of the transistor we will have

$$\frac{\Delta I_C}{I_C} \simeq 2 \frac{\Delta \beta}{\beta^2} \, .$$

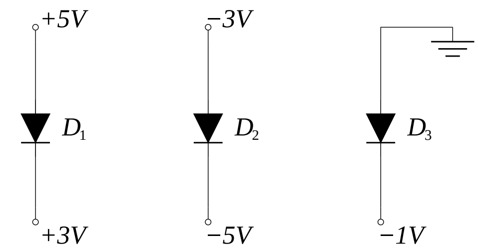
In other words, the stability of this current source due to the fluctuations of the transistor properties are expected to be remarkably good. In fact, if we suppose to have $\beta = 100$ and change of 100% in β then

$$\left\{ \begin{array}{rcl} \beta & = & 100 \\ \Delta\beta & = & 100 \end{array} \right. \qquad \Rightarrow \frac{\Delta I_C}{I_C} \simeq 0.02$$

For their simplicity, current mirror are extensively used in ICs design where a constant current source is needed.

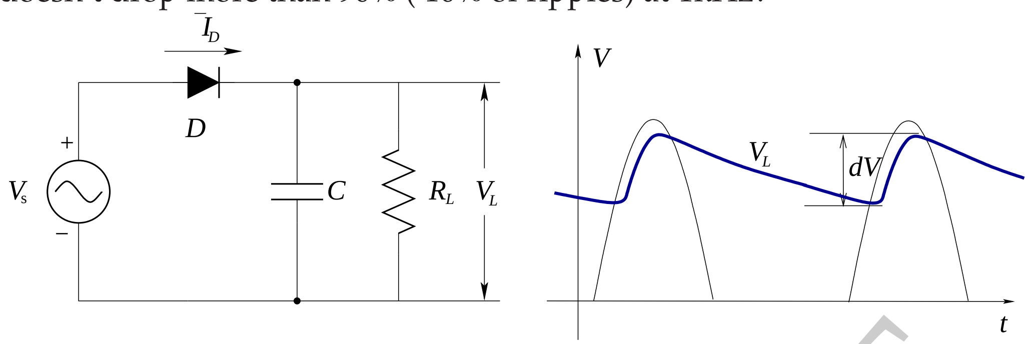
2.6 Pre-Laboratory Problems

1. Considering the following Figure, state which cases have the diode conducting



2. Calculate the resistance R needed to limit the current flowing through a diode to 10mA with a voltage source of $V_s = 5$V.

3. Adding a Capacitor C in parallel to the the half-wave rectifier load R_L we low-pass filter the rectifier. If the load $R_L = 1$kΩ, what must be the value of the capacitor C (within 10%) so the voltage output doesn't drop more than 90% (10% of ripples) at 1kHz?



(Hint: consider that the capacitor is just discharging through the load R_L).

4. Supposing that we want a maximum current of 1mA going through the base, and the maximum applied input voltage $V_{i,max}$ is 5V, determine the value of R_B for the BJT switch circuit. Considering that $V_{i,max}$ is 5V , what is a possible and practical V_{CC} value that allows the BJT to work in saturation mode ? Once found such a value of V_{CC} , determine the R_C resistor value to limit the I_C current to 1 mA when the BJT is saturation mode.

5. Estimate the β of the npn transistor 2N2222 in Figure 2.10. Determine

the values of R_B, and R_C for the BJT amplifier when $V_{CC} = 15$ V, $\beta = 200$, and a value of I_B between 50 μA and 100 μA.

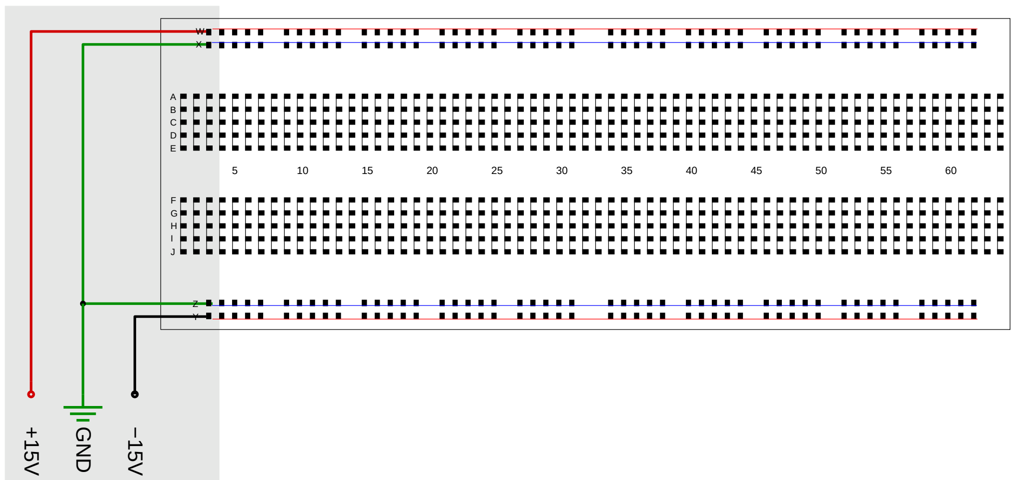


Figure 2.18: Electronic circuit breadboard contacts topology and suggested connections. Power supplies voltage distribution and LED connections are highlighted with gray boxes. Whenever possible black jacket wires should be used to connect components to ground (GND) , red jacket wires for $+15V$ and white jacket wires for $-15V$. This pragmatism helps debugging the circuit.

2.7 Procedure

Remember to consult the components data-sheets to properly connect diodes and transistors leads.

It is good practice to check the power supply connections before turning generators or sources on.

1. Using the half-wave rectifier circuit and the data acquisition, plot the volt-ampere characteristic of a silicon, and a germanium diode. Use channel 1 to measure the voltage drop across the diode and channel 2 for voltage across the resistor. Choose R to limit the current to a maximum of 10mA.

2. With a 1kHz sinusoidal signal verify the response of the previously built half-wave rectifier comparing the rectifier output with the voltage source signal. Then connect a capacitor in the proper way to obtain ripples of about 10% of the maximum output voltage.

3. Build a BJT switch working with the TTL logic levels $ON \Rightarrow\sim$ 5V and $OFF \Rightarrow\sim$ 0V.
   Check the status of the two junctions measuring the voltage drop across them for the cut-off and the saturation mode.
   Connecting two silicon diodes to the BJT switch input in a proper way implement a NOR GATE, i.e. a circuit with two inputs A and B and one output C which fulfills the following true table:

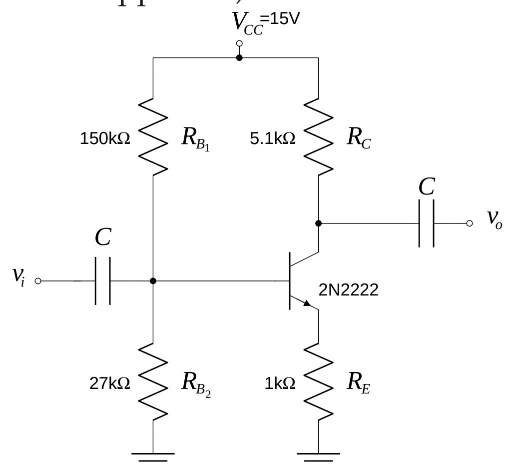
A	B	$A\ OR\ B$	$C = \overline{A\ OR\ B}$
OFF	OFF	OFF	ON
OFF	ON	ON	OFF
ON	OFF	ON	OFF
ON	ON	ON	OFF

   Hint: one lead of each diode should be connected to the switch input. Explain why the diodes are needed.

4. Build the Simple BJT amplifier explained in section 2.5.4 using a 2N2222 transistor, and do the following steps

   (a) Check the DC bias V_{CE} and V_{BE} of the two BJT junctions,
   (b) measure the transfer function, and find the two cutoff frequencies where the amplitude is -3dB down from the plateau,
   (c) download the simulation file from the ph5/105 website for the circuit, input the proper components values,
   (d) run the DC operating point simulation to check the transistor working point,
   (e) run the AC response simulation and find eventual discrepancies beteween your measurement and the simulation,
   (f) run the transient response and compare teh result with the real response of the circuit

5. Optional: Build the following common emitter amplifier circuit (the circuit is explained in the appendix)



and do the following steps

(a) Check the DC bias V_{CE} and V_{BE} of the two junctions .

(b) Measure the transfer function, and find the two cutoff frequencies where the amplitude is -3dB down from the plateau.

(c) Verify that the transfer function plateau has a gain $|G| \simeq R_C/R_E$.

(d) download the simulation file from the ph5/105 website for the circuit, input the proper components values,

(e) run the DC operating point simulation to check the transistor working point,

(f) run the AC response simulation and find eventual discrepancies beteween your measurement and the simulation,

(g) run the transient response and compare teh result with the real response of the circuit

Bibliography

[1] ??Find a reference to Regulators??

[2] Microelectronics, Jacob Millman & Arvin Grabel, McGraw-Hill Electrical Engineering Series.

[3] The art of Electronics Second Edition, Paul Horowitz & Winfield Hill, Cambridge University Press

Chapter 3

The Operational Amplifier

3.1 Introduction

Operational amplifiers are one of the most extensively used analog integrated circuits especially because of their ability to approximate reasonably well the ideal behavior. For this reason, real operational amplifiers can be quite often modeled as ideal or quasi-ideal. Moreover, the versatility this device, which hides a large internal complexity [1], makes the operational amplifier suitable for many different applications.

In the first section, the mathematical formulation makes the ideal operational amplifier concept quite awkward, especially after a first reading. Using the ideal device properties in conjunction with the so called feedback network, which links the output of the amplifier inputs, will clarify the definition of the ideal operation amplifier.

The subsequent section is dedicated to the explanation of some basic operational amplifier circuits. Finally, section 3.4 introduces a more realistic model of operational amplifier together with some of the particular behavior of this electronic device.

[1]A modern operational amplifier made of a cascade of stages, each one designed mainly to match the ideal characteristics, can have around 50 components both active and passive. See the Analog Devices Web site, for example.

3.2 The Ideal Operational Amplifier

The ideal operational amplifier (Op-Amp) is a linear amplifier with two differential inputs v_+, v_- and one output v_o (see figure 3.1) and with the following characteristics:

- $v_0 = A_v(v_+ - v_-), \qquad A_v > 0$, (linearity)
- input resistance $R_i \to \infty$,
- output resistance $R_o \to 0$,
- voltage gain $A_v \to \infty$,
- frequency response constant for any frequency.

Aside the welcome property of linearity and infinite frequency response, the need of all the other characteristics can be justified as follows. Infinite input resistance R_i means essentially that the Op-Amp inputs do not produce perturbations to any circuit to which they are connected to. Zero output resistance R_o perfectly isolates the Op-Amp from any perturbation. Infinite input impedance and zero output impedance implies also no dissipation of energy. The condition of infinite voltage gain A_v is necessary if we want a device able to deliver any gain, once a network which connects the output to the input is added to the Op-Amp. In general, this kind of network is called *feedback network*.

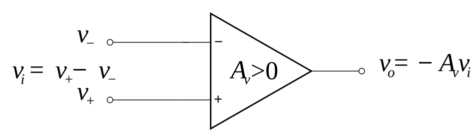


Figure 3.1: Op-Amp symbol, and some definitions of variables.

3.2.1 Ideal Op-Amp Fundamental Equation (Golden Rules)

The consequence of the following conditions

- $A_v \to \infty$,
- $v_o < \infty$ if $v_i = v_+ - v_- < \infty$,

is the following very useful and important formula

$$v_+ - v_- = 0, \qquad \text{at all times.} \tag{3.1}$$

Equation 3.1 will be called the *first Op-Amp golden rule.*

The consequence of the following condition

- $R_i \to \infty$,

is

$$i_+ - i_- = 0, \qquad \text{at all times,} \tag{3.2}$$

Equation 3.2 will be called the *second Op-Amp golden rule*.

These two rules are fundamental for the solution of any circuit involving Op-Amps. We will see in the next sections the importance of this equations once a feedback network is connected to the Op-Amp.

3.2.2 Op-Amp Input Output "Logic"

It is worthwhile here to notice the behavior of Op-Amp output as function of the two inputs. From the definition of Op-Amp we have that a signal sent to the negative input V_- is amplified and changed in sign. A signal sent to the positive input V_+ is just amplified. Two signals sent each to one input are indeed subtracted and amplified.

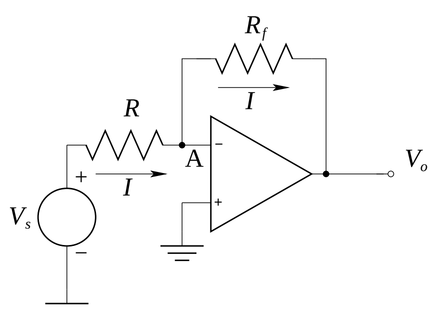


Figure 3.2: Op-Amp with a feedback network.

3.2.3 Op-Amp with a Feedback Network

Let's consider the circuit in figure 3.2, where a feedback resistance R_f is connected to the negative input. The current through the resistors R and

R_f is the same because the ideal Op-Amp input does not drive any current ($R_i = \infty$). Furthermore, since $V_i = V_+ - V_- = 0$ and with the use Ohm's law and the KVL, it follows that

$$I = \frac{V_s}{R} = -\frac{V_o}{R_f}. \tag{3.3}$$

The output voltage V_o and voltage gain A will be

$$V_o = AV_s, \qquad A = -\frac{R_f}{R}.$$

The gain of the Op-Amp depends just on the resistances ratio R_f and R.

3.2.4 The Virtual Ground

Let's re-analyze the circuit in figure 3.2. Considering that the golden rule imposes $V_i = V_+ - V_- = 0$, and the negative input is grounded, the node **A** must always be at zero voltage. This is equivalent to having **A** virtually grounded. The adjective virtual is necessary because even if **A** is at the potential of the ground there is no current flowing through **A** ($R_i = \infty$) as in a real ground**.** In other words, the virtual ground happens to be because the Op-Amp does its best to keep $V_i = 0$.

3.3 Commonly Used Op-Amp Circuits

In the study of the several common Op-Amp configurations, we will use the approximation of an ideal circuit. A more realistic model is often necessary to understand some behaviors of real circuits. For an initial design, and where the the ideal Op-Amp characteristics are well approximated, the ideal model is quite often sufficient.

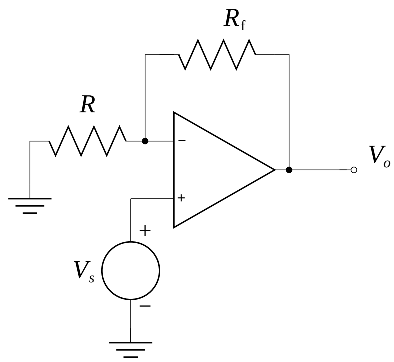


Figure 3.3: Non-inverting configurations of the Op-Amp.

3.3.1 Non-Inverting Amplifier

Let's consider the non-inverting configuration of the Op-Amp in figure 3.3. Because of $V_i = 0$, we will have

$$V_s - V_- = V_s - RI = 0.$$

Considering that the output voltage V_o is

$$V_o = (R_f + R)I,$$

we can use the expression of I to obtain

$$V_s = \frac{R}{R + R_f} V_o.$$

The output voltage V_o and voltage gain A will be

$$V_o = AV_s, \qquad A = 1 + \frac{R_f}{R}.$$

Considering that in this configuration V_s is directly connected to $V_+$and V_- is not a virtual ground, the input impedance of the amplifier is $R_i + R$, where R_i is the real input impedance of the Op-Amp.

3.3.2 Inverting Amplifier

This circuit has been already discussed in section 3.2.3. For completeness, the solution and some comments are here reported

$$V_o = AV_s, \qquad A = -\frac{R_f}{R}.$$

It is worthwhile to notice that because $V_- = 0$, the circuit input impedance is just R. Having values of R typically of few $k\Omega$, the inverting configuration doesn't preserve the high impedance characteristic of an Op-Amp. A connection of the circuit input to a network can potentially create appreciable perturbations.

3.3.3 Differential Input Stage

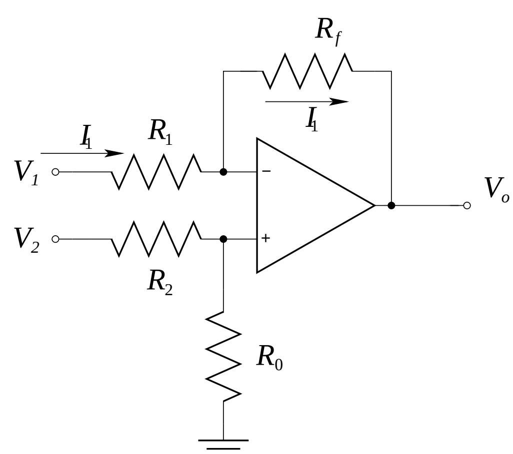


Figure 3.4: Differential input configuration of the Op-Amp.

Let's now solve the differential input circuit of the Op-Amp in figure 3.4.

Writing the voltage drop across $R_1$and R_f, we obtain the linear system

$$\begin{aligned} V_- - V_1 &= R_1 I, \\ V_o - V_- &= R_f I. \end{aligned}$$

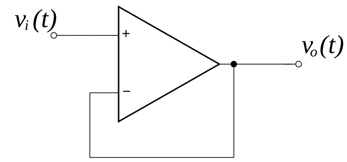


Figure 3.5: Voltage follower or unity gain buffer.

Solving the system with respect to V_o, we get

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_- - \frac{R_f}{R_1} V_1.$$

Using the voltage divider equation to obtain $V_+$and because $V_+ - V_- = 0$, we have

$$V_- = V_+ = \frac{R_0}{R_2 + R_0} V_2,$$

and finally, we get

$$V_o = \frac{R_1 + R_f}{R_1} \frac{R_0}{R_2 + R_0} V_2 - \frac{R_f}{R_1} V_1.$$

A way to to obtain the same voltage gain for V_2 and V_1 is to impose $R_0 = R_f$ and $R_1 = R_2 = R$. The output voltage becomes

$$V_o = A(V_2 - V_1), \qquad A = \frac{R_f}{R}.$$

This differential configuration is not very convenient because it does not preserve the high input impedance of the Op-Amp. In fact , considering that the Op-Amp input impedance is very high, we have that the resistance seen from V_1 is $R_2 + R_0$. Usually, the sum of those resistors is at least one order of magnitude smaller than the Op-Amp input impedance. If we need to build a variable gain differential amplifier, we will need to change more than one resistor value. Matching the resistances values can become an issue when thermal drifts become important.

More practical and stable configurations called instrumentation amplifiers are available “off the shelf”.

3.3.4 Voltage Follower (Unity Gain "Buffer")

The circuit sketched in figure 3.5 is called voltage follower or unity gain buffer. The feedback line with no load gives

$$v_o(t) = v_-.$$

Moreover, because of the golden rule we will have

$$v_- = v_+,$$

which implies

$$v_o = v_i.$$

The output voltage $v_o(t)$ follows the input voltage $v_i(t)$ with unitary gain.

Considering that the high impedance input and the low impedance output values of Op-Amps are close to the state of the art in the electronic design[2], the voltage follower can be used as an isolation stage (buffer) between two circuits.

3.3.5 Integrator Amplifier

Let's consider the circuit in figure 3.6 without the resistance R_f. The voltage drop v_o across the capacitor C_f is

$$v_o(t) = -\frac{1}{C_f}\int_{-\infty}^{t} i(\tau)d\tau \tag{3.4}$$

and the current flowing through the resistance R is

$$i(t) = \frac{v_i(t)}{R}.$$

[2]Devices expressly made to work as input unity gain buffer, and output unity gain buffer are also available. Analog Devices SSM2141 and SSM2142 are complementary buffers devices which can drive long delay lines for example.

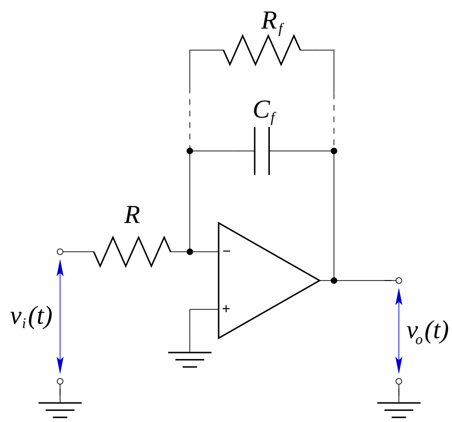


Figure 3.6: Active integration stage using an Op-Amp.

Placing the expression of $i(t)$ obtained from the previous equation into eq.(3.4), we will obtain

$$v_o(t) = -\frac{1}{\tau} \int_{-\infty}^{t} v_i(t')dt', \qquad \tau = RC_f.$$

Real Op-Amps or signals connected to the input have often (always) a DC offset. This offset is indeed integrated and after a given time will saturate the amplifier output. This saturation is essentially a manifestation of the instability of the circuit at low frequency. Moreover, the initial charge of the capacitor is undefined, making the initial output state unpredictable.

A common way to avoid these problems is to introduce the resistance R_f in parallel with the capacitor C_f which reduces the amplifier DC gain. An intuitive way to understand the effect of this feedback resistance is that it does not allow the capacitor to be charged "ad libitum". The choice of the R_f is not so trivial if we want to preserve the characteristic of good integrator. Using the simple phasor analysis it easy to prove that the good integrator condition is $\omega \gg 1/C_f R_f$.

If the DC current must be integrated, we can place a switch in parallel with the capacitor to be opened when the integration is started. In this way we will have the capacitor state completely defined.

3.3.6 Differentiator Amplifier

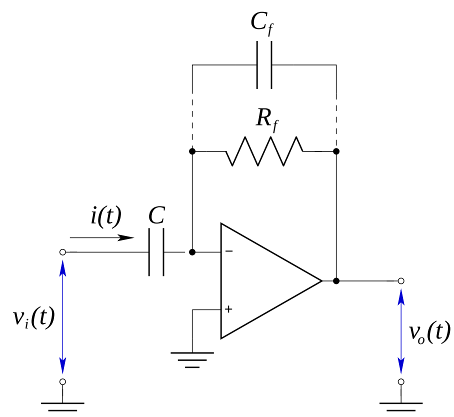


Figure 3.7: Differentiator stage using an Op-Amp.

Let's now consider the circuit in figure 3.7 without the feedback capacitor C_f. Applying a similar analysis to that used in the integrator amplifier we will have

$$\begin{aligned} i(t) &= C\frac{dv_i}{dt}, \\ v_o(t) &= -R_f i. \end{aligned}$$

and indeed

$$v_o(t) = -\tau\frac{dv_i}{dt}, \qquad \tau = R_f C.$$

This configuration without C_f doesn't work well with real Op-Amps, because of stability problems. In fact, the introduction of the capacitor compromises the internal compensation of the Op-Amp. Placing a capacitor C_f in the feedback network restores the compensation making the overall circuit stable. The choice of C_f is not trivial if we want to preserve the circuit differentiator characteristics.

Section 3.4.3 explains in more details the effect of this configuration on the compensation of a real Op-Amp.

3.4 The Real Op-Amp

Lets consider in this section a more realistic model of the Op-Amp by including a finite input impedance R_i, non zero output impedance R_o, finite gain A, bias currents and voltage offsets. Using ideal components, the equivalent circuit of the real Op-Amp is shown in figure 3.8.

3.4.1 Bias Currents and Voltage and Current Offsets

Imbalances inside of the Op-Amp, mainly due to differences in the electronics components, produce undesirable bias currents and a voltage offset at the inputs. Input voltage and current offsets can be modeled by introducing ideal generators as shown in figure 3.8. Current Offset is defined as the difference in the magnitude of the bias currents, i.e.

$$i_{os} = |i_{b+}| - |i_{b-}|$$

A way to characterize the voltage offset is to use the voltage follower configuration (see section 3.3.4) with the input V_i connected to the ground. The voltage offset will be directly the output voltage V_o.

Current input biases can be studied connecting a resistor between the one input and ground and measuring the voltage drop across the resistor.

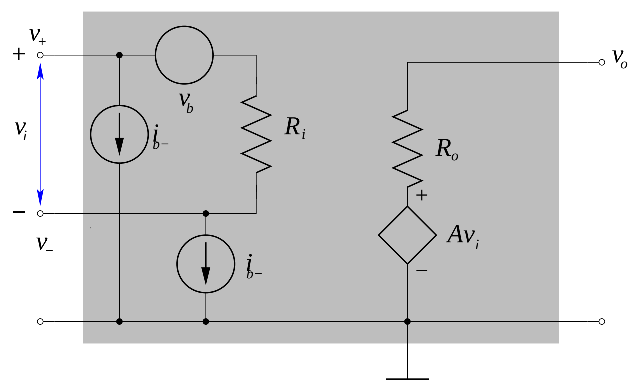


Figure 3.8: Equivalent circuit for an Op-Amp using ideal components. Voltage offsets and current biases are taken into account using ideal voltage and current generators.

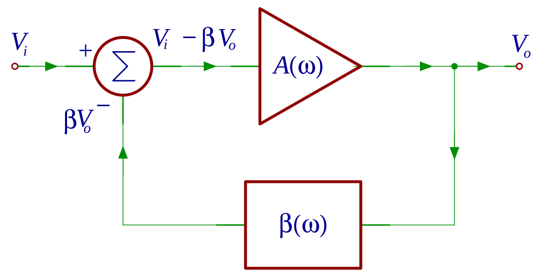


Figure 3.9: Amplifier with negative feedback.

3.4.2 Feedback Amplifiers

Let's consider an amplifier with a negative feedback network as show in figure 6.1. Considering that the summation point output is

$$V_i - \beta(\omega)V_o\,,$$

and the amplifier gain is $A_{OL}(\omega)$, the output voltage will be

$$V_o = A(V_i - \beta V_o)\,.$$

Collecting V_o, we will have

$$V_o = \frac{A}{1+\beta A}V_i\,,$$

and the so called *closed loop transfer function*, A_{CL}, will finally be

$$A_{CL}(\omega) = \frac{A}{1+\beta A}\,. \tag{3.5}$$

We can clearly see that if the denominator goes to zero for a given frequency ω^*, we are in trouble, $A_{CL}(\omega^*)$ diverges, and the amplifier saturates. The trick to avoid this situation, is to study the following equation

$$A_{OL}(\omega) = \beta(\omega)A(\omega) = -1, \tag{3.6}$$

where A_{OL} is the *feedback amplifier open loop transfer function*. If the phase where the magnitude of $A_{OL}$is equal to one is different from 180^0plus multiples of 360^0, the denominator never goes to zero and the saturation is avoided. However, this is not enough because we can have just an oscillation with no saturation if the A_{OL} phase is too close to 180^0. The rule of thumb is to have a so called phase margin of about $60^0$from 180^0. Finally, we can formulate the criterion for the stability:

$$\text{where } |A_{OL}| = 1 \qquad \Rightarrow -120 < \arg(A_{OL}) < 120\,.$$

Another important result of the theory of feedback amplifier is the following straightforward result

$$\text{if} \quad \beta A \gg 1 \qquad \Rightarrow \qquad A_{CL}(\omega) \simeq \frac{1}{\beta}\,.$$

Where the open loop transfer function $A\beta$ is greater than one the feedback amplifier response does not depend on the response $A(\omega)$ of the amplifier with no feedback. It is worthwhile to notice that the ideal amplifier ($A \to \infty$) has $A_{CL} = 1/\beta$ for all angular frequencies. A close loop ideal amplifier does not have undesired instabilities, but just the ones that can be introduced by the feedback network.

3.4.2.1 Non-Inverting Configuration

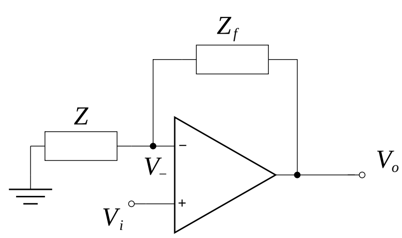


Figure 3.10: Non-inverting configuration Op-Amp with generic impedance.

Considering the Op-Amp Non-Inverting configuration as shown in figure 3.10, and the voltage divider equation we have

$$V_- = \frac{Z}{Z_f + Z} V_o\,, \tag{3.7}$$

and the feedback network transfer function is

$$\beta(\omega) = \frac{V-}{V_0} = \frac{Z}{Z_f + Z}\,.$$

The approximate gain of the feedback amplifier is as expected

$$A_{CL} \simeq \frac{1}{\beta} = 1 + \frac{Z_f}{Z}.$$

3.4.2.2 Inverting Configuration

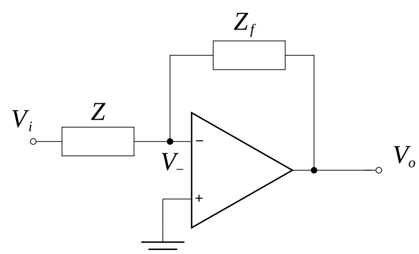


Figure 3.11: Inverting configuration Op-Amp with generic impedance.

In this case the feedback network transfer function β is

$$\beta = \frac{V_i}{V_0}$$

Considering the inverting configuration stage as shown in figure 3.11, because of the virtual ground we have

$$\begin{cases} V_i &= ZI \\ -V_o &= Z_f I \end{cases} \Rightarrow \quad \beta(\omega) = -\frac{Z}{Z_f},$$

and the gain of the feedback amplifier is simply

$$A_{CL} \simeq \frac{1}{\beta} = -\frac{Z_f}{Z}.$$

3.4.3 Compensated Op-Amp Transfer Function

Practical Op-Amps are often designed to have a frequency response dominated by a single pole, i.e. the transfer function with no feedback is just a simple low-pass filter. In this case, the Op-Amp transfer function with no feedback can be written as

$$A(\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_0}}, \tag{3.8}$$

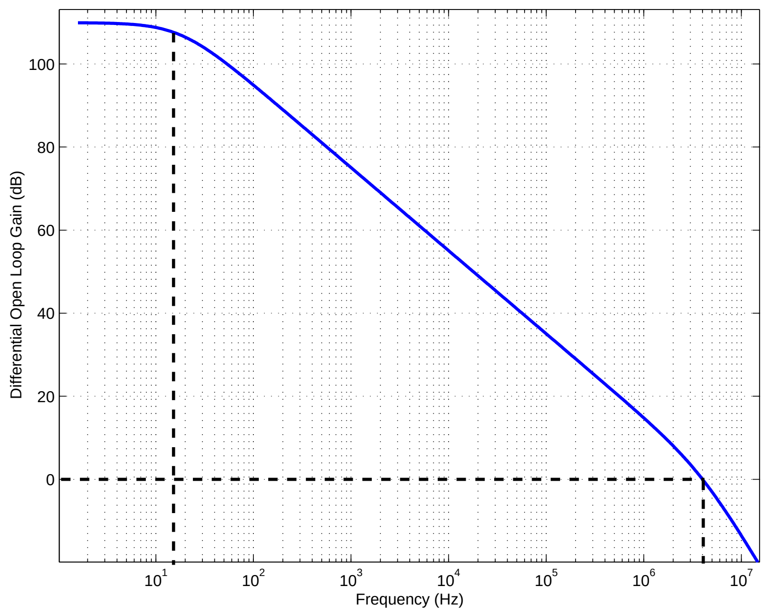


Figure 3.12: Differential gain of the AD711 Op-Amp (cut-off frequency $\nu_0 = 18$Hz, unity gain frequency $\nu_1 = 4$MHz, and DC gain $a_0 = 110$dB). Dominant single pole behavior is valid up to about 4MHz, where the slope becomes steeper than $1/\omega$.

where A_0 is the DC gain and ω_0 is the angular frequency of the dominant pole (the cut-off angular frequency of the low pass filter). This behavior is obtained by introducing a compensating circuit (quite often a capacitor) in the architecture of the Op-Amp.

This choice comes from the stability requirement that we mentioned in the previous section. In fact, an amplifier with a transfer function with a dominant pole cannot lose more than 90^0 making quite easy the design of a stable feedback network. For example, feedback networks with just resistors, (ideal resistors don't loose phase) will not generate oscillations.

Typical values for pole frequencies are between 5Hz and 100Hz. Figure 3.12 shows the differential transfer function of the Op-Amp AD711 with no feedback network.

Let's study more in details the compensated Op-Amp response with a feedback.

3.4.4 Compensated Op-Amp with Constant Frequency Response Feedback

Considering the frequency response of a compensated feedback amplifier, we will have

$$\begin{aligned} A(\omega) &= \left(\frac{A_0}{1+j\frac{\omega}{\omega_0}}\right) \Big/ \left(1+\frac{\beta A_0}{1+j\frac{\omega}{\omega_0}}\right), \\ &= \frac{A_0}{1+\beta A+j\frac{\omega}{\omega_0}}, \\ &= \left(\frac{A_0}{1+A_0\beta}\right) \Big/ \left(1+j\frac{\omega}{\omega_0(1+\beta A_0)}\right). \end{aligned}$$

In the particular case that $\beta(\omega)$ is constant and $\beta = \beta_0 \geq 1$, the previous equation becomes

$$A(\omega) = \frac{A_1}{1+j\frac{\omega}{\omega_1}}, \qquad \begin{cases} A_1 &= \frac{A_0}{1+A_0\beta_0} \\ \omega_1 &= \omega_0(1+\beta_0 A_0) \end{cases}$$

In this case, the feedback Op-Amp response is the same as of the open loop transfer function A_{OL}but with a smaller DC gain (about $1/\beta_0$) and higher cut off angular frequency ω_1 $\omega_0\beta_0 A_0$.

3.4.5 Compensated Op-Amp in the Differentiator Configuration

Let's find the frequency response of the "real" Op-Amp differentiator circuit of figure 3.7. For the basic differentiator (no capacitor C_f) the feedback network transfer function is

$$\beta = -\frac{Z}{Z_f} = -\frac{1}{j\omega RC} = j\frac{\omega_1}{\omega}, \qquad \omega_1 = \frac{1}{RC}.$$

Considering eq. (3.5), we have that the gain of the differentiator is

$$A_{CL}(\omega) = \frac{A(\omega)}{1+jA(\omega)\,\omega_1/\omega} = \frac{1}{1/A+j\,\omega_1/\omega},$$

and finally

$$A_{CL}(\omega) = \frac{A_0}{1 + j\left(A_0\frac{\omega_1}{\omega} + \frac{\omega}{\omega_0}\right)} = -A_0\omega_0\frac{j\omega}{\omega^2 - j\omega\omega_0 + A_0\omega_0\omega_1}.$$

Resonance occurs when the denominator goes to zero, i.e for

$$\omega^* = j\frac{\omega_0}{2} \pm j\sqrt{\frac{\omega_0^2}{4} + A_0\omega_0\omega_1} \simeq \pm j\sqrt{A_0\omega_0\omega_1}, \qquad \omega_0 \ll \omega_1,\ A \geq 1.$$

3.4.6 The Common Mode Rejection Ratio (CMRR)

We want characterize the rejection of an Op-Amp output as a differential amplifier, of signals sent to both inputs. For an ideal Op-Amp we expect to obtain $V_o = 0$ for all frequencies, i.e. a perfect rejection. To define a convenient parameter which measures the rejection it is necessary to define the following ones, the *common mode gain*

$$A_C(\omega) = \frac{V_o}{V_+ - V_-}, \qquad V_+ = V_- = V_s\sin(\omega t),$$

and the *differential mode gain*

$$A_D(\omega) = \frac{V_o}{V_+ - V_-}, \qquad V_+ = V_s\sin(\omega t), \quad V_- = 0.$$

The *Common Mode Rejection Ratio (CMRR)* is defined as the modulus of the ratio of the differential gain A_D over the common mode gain A_C, i.e.

$$CMRR(\omega) = \left|\frac{A_D(\omega)}{A_C(\omega)}\right|$$

Ideally, the $CMRR$ should be infinity for all frequencies.

This parameter can be measured using the Op-Amp differential configuration (see figure 3.4) and measuring A_C and A_D as a function of the frequency. To minimize possible large systematic errors, it is necessary to have the same gain for the to inputs V_1 and V_2. This can be achieved by placing a trimmer in the voltage divider mesh of the differential configuration circuit. Adjusting the trimmer we can minimize V_o for a single frequency and study the $CMRR$ for a given bandwidth.

Figure 3.13shows the $CMRR$ as a function of frequency of a typical Op-Amp. A typical value for $CMRR$ is 90dB.

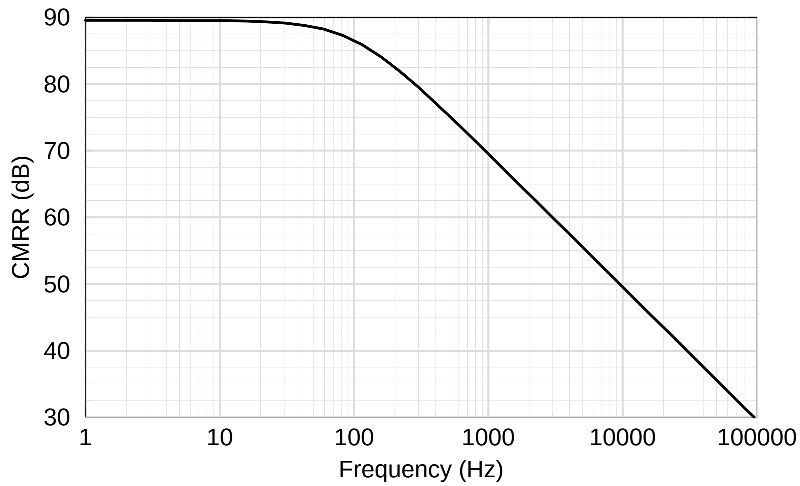


Figure 3.13: *CMRR* as a function of frequency of a typical Op-Amp.

3.4.7 The Gain Bandwidth Product (GBWP)

The gain bandwidth product is a common way to characterize the gain with respect to the available bandwidth of amplification. It is defined as

$$GBWP = A_0\omega_0.$$

The larger the GBWP the better is the Op-Amp, and the closer the Op-Amp is to the ideal operational amplifier.

3.4.8 The Slew Rate (SR)

The *slew rate* or *maximum slew rate* SR of an Op-Amp is defined as the maximum rate of the output voltage v_o per unit time

$$SR = \max\left\{\left|\frac{\Delta v_o(v_i)}{\Delta t}\right|\right\}.$$

This parameter essentially measures the ability of an Op-Amp to follow voltage changes for large voltage inputs.

The slew rate can be easily observed sending a square wave (see figure 3.14) to the Op-Amp input v_i, and looking at the raising and falling slope of the output signal v_o. If the slopes do not change changing the input amplitude, then the Op-Amp is slew rate limited.

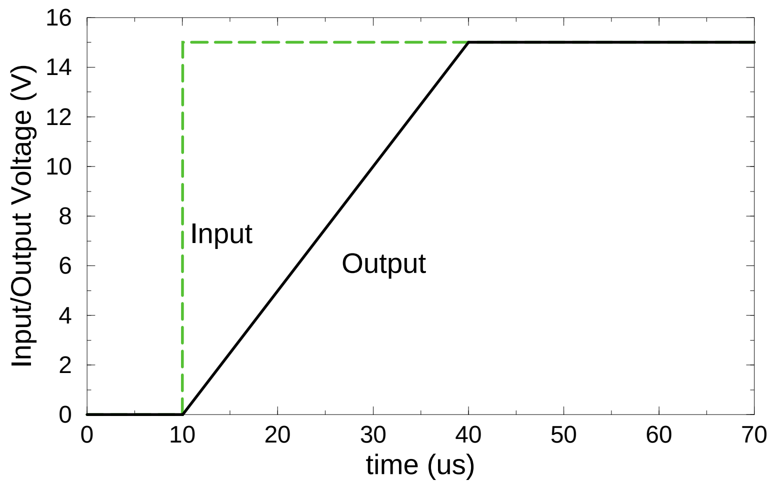


Figure 3.14: Slew rate illustration. The output v_o takes 40μs to reach the desired voltage. The device is said to be slew rate limited.

A similar procedure can be applied using a low frequency sinusoidal signal as input. In this case if we increase the input amplitude too much, the output will become distorted. Considering a sinusoid of frequency $\omega_0$and amplitude V_o

$$SR = \max\left\{\left|\frac{d}{dt}V_o \sin\,\omega_0 t\right|\right\} = \omega_0 V_o \max\left\{\cos\,\omega_0 t\right\} = \omega_0 V_0.$$

For an undistorted signal with amplitude V and maximum frequency ω, we must have

$$SR \gg \omega V\ .$$

Usually, a frequency compensated Op-Amp has a passive integrating stage at the output, and therefore the slew rate is often proportional to the inverse of the capacitance of the compensating network.

Typical good slew rate values are of the order of few V/μs.

3.4.9 Ideal versus Real and Practical Considerations

The following table summarizes the main characteristic of an ideal Op-Amp together with those of typical real Op-Amp. In some cases we can find Op-Amps excelling some of the mentioned characteristics , quite often at the expense of other characteristics.

Property	Ideal Op-Amp	Typical Op-Amp
Open-Loop DC Gain A_v	∞	$> 10^4$
Open-Loop Bandwidth	∞	$\sim$ 10Hz (dominant pole)
Common Mode Rejection Ratio $CMRR$	∞	> 70dB
Input Resistance R_i	∞	> 10MΩ
Output Resistance R_o	0	$< 500\Omega$
Input Current $\delta I_\pm$	0	$< 0.5\mu$A
Input Offset Voltage $\delta V_\pm$	0	< 10mV
Input Offset Current δI_i	0	< 200pA

What are the conditions that dictate the range of the feedback impedances R_f? Apart from special cases, the feedback current I should be only a small fraction of the maximum output current I_o, i.e. $I = 1\% I_o$. A typical Op-Amp has a maximum output of 10mA at 10V, i.e.

$$R_f = \frac{V}{I} = \frac{10\text{V}}{10 \cdot 1\%\text{mA}} = 100\text{k}\Omega$$

Typical feedback resistors should be in the range of $R_f = 50 - 1\text{M}\Omega$.

Small difference on the differential stage of the Op-Amp produces a DC offset δV at the input, which can produce large DC output if the gain is extremely high. For example, if we have

$$\delta V = 10\text{mV}, \quad G \geq 10^4, \Rightarrow V_o \geq 10V.$$

3.5 Problems Preparatory to the Laboratory

1. Supposing that the open-loop gain of an Op-Amp is a simple low pass filter (first order) with DC gain 144dB and cut-off frequency $f_0 = 10$Hz, sketch in a bode diagram, the magnitude of the frequency response of a non-inverting stage with gain $G = 10$ at 10Hz.

2. Prove that the good integrator condition for the circuit in figure 3.6 is $\omega \gg 1/R_f C_f$. (Hint: calculate the response of the circuit and compare it with the ideal response of the ideal inverting integrator, i.e. $A(\omega) = -1/(j\omega RC)$. Calculate the DC gain of the integrator transfer function.

3. Using an integrator stage with a feedback resistor R_f, and time constant $\tau = RC$, compute the values for τ and R_f needed to integrate a sinusoidal wave with frequency $f > 1$kHz and with 10% of losses in the integration. Choose a value of $R \gg R_s$, where $R_s = 50\Omega$ is the input impedance of the used function generator.

4. Show that the slope of an integrated square wave is the inverse of of the time constant $\tau = RC_f$ of the Integrator shown in figure 3.6. Which characteristics of the square wave are needed to fulfill the requirement to not saturate the integrator output ?

5. Consider a differential stage having the following resistances values: $R_1 = R_2 = 50\,\text{k}\Omega$, $R_f = R_0 = 100\ \text{k}\Omega$. Calculate the following quantities

   (a) the two input impedances $Z_1$and Z_2 ,

   (b) the output impedance Z_o,

   (c) Considering that the Op-Amp max output current and voltage are respectively I_{max} =10mA and $V_{max} = 10$V, calculate the smallest load R_{min} it can drive .

3.6 Laboratory Procedure

Read carefully the entire procedure before starting the experiment, and note on your log book all the unpredicted behavior you experience in the circuits response.

Consult the data-sheet to properly map the μ741 and AD711 Op-Amp pin-out.

Op-Amp output high frequency noise can be reduced by adding 100nF capacitors closest as possible to the $\pm 15V$ power supplies input of the Op-Amp.

Before powering your circuit up, cross-check the power supply connections.

It is always a good practice to turn on the power supplies at the same time to avoid potential damages of the Op-Amps.

Using the μ741 Op-Amp, do the following steps:

- Using a non-inverting configuration with a gain of 100, verify the transfer function of the Op-Amp.
- Using the same previous circuit, estimate the slew rate of the Op-Amp. Redo the same measurement using an AD711 Op-Amp.
- Study the $CMRR$ using a differential configuration. Use a potentiometer to balance the gains at just one frequency and then measure the $CMRR$. Verify that the obtained values are in agreement with the specifications reported in the Op-Amp data-sheet. Mount and tune the null adjustment circuit as specified in the Op-Amp data-sheet.

Build an integration stage using an Op-Amp having a time constant $\tau \sim 100\mu s$. Include a feedback resistor R_f to avoid saturation at the output and do the following steps:

- Measure the impulse response.
- Measure the frequency response.
- Estimate the integrator time constant τ using a square wave.

Bibliography

[1] The Art of Electronics, Paul Horowitz and Winfield Hill, Cambridge University Press.

[2] Microelectronics Jacob Millman & Arvin Grabel, McGraw-Hill Electrical Engineering Series

[3] Analog Devices web site www.analog.com AD625: Programmable Gain Instrumentation Amplifier Data Sheet (Rev. D, 6/00).

[4] An Introduction to Operational Amplifiers with Linear IC, Second Edition, Luces M. Faulkenberry, edited by John Wiley and Son.

Chapter 4

Basic Op-Amp Applications

4.1 Introduction

In this chapter we will briefly describe some quite useful circuit based on Op-Amp, bipolar junction transistors, and diodes.

4.1.1 Inverting Summing Stage

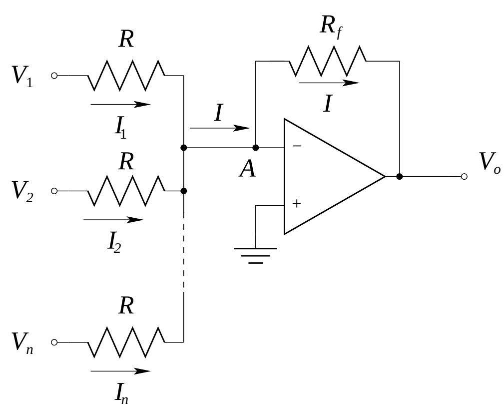


Figure 4.1: Inverting summing stage using an Op-Amp. The analysis of the circuit is quite easy considering that the node A is a virtual ground.

Figure 4.1 shows the typical configuration of an inverting summing stage using an Op-Amp. Using the virtual ground rule for node A and

Ohm's law we have

$$I_n = \frac{V_n}{R}, \qquad I = \sum_{n=1}^{N} I_n.$$

Considering that the output voltage V_0 is

$$V_o = -R_f I,$$

we will have

$$V_o = A \sum_{n=1}^{N} V_n, \qquad A = -\frac{R_f}{R}.$$

4.1.2 Basic Instrumentation Amplifier

Instrumentation amplifiers (In-Amp) are designed to have the following characteristics: differential input, very high input impedance, very low output impedance, variable gain, high CMRR, and good thermal stability. Because of those characteristics they are suitable but not restricted to be used as input stages of electronics instruments.

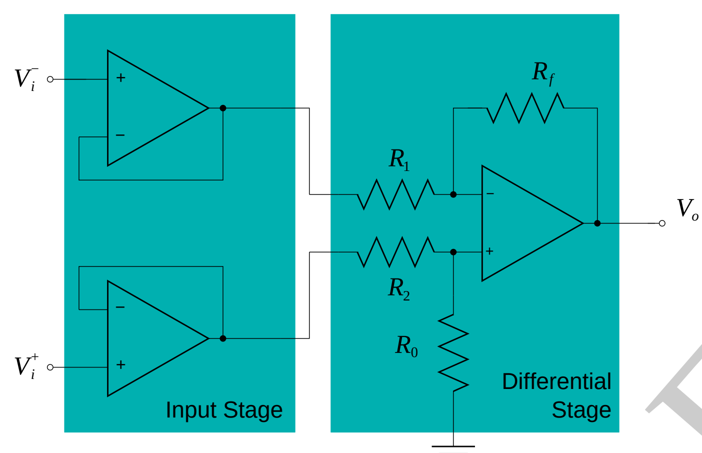
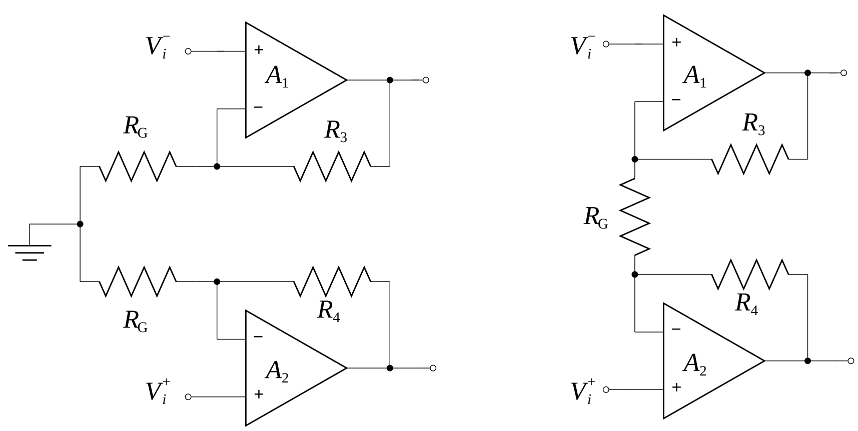


Figure 4.2: Basic instrumentation amplifier circuit.

Figure 4.2 shows a configuration of three operational amplifier necessary to build a basic In-Amps. The two buffers improve the input impedance of this In-Amp, but some of the problems of the differential amplifier are still present in this circuit, such as common variable gain, and gain thermal stability.

A straightforward improvement is to introduce a variable gain on both amplifiers of the input stage as shown in Figure 4.3(a). Unfortunately, it is quite hard to keep the impedance of the two Op-Amps well matched, and contemporary vary their gain to keep a very high CMRR. A clever solution to this problem is shown in Figure 4.3(b). Because of the virtual ground this configuration is not very different from the previous one but it has the advantage of requiring one resistor to set the gain. In fact, if $R_1 = R_4$ then the gain of the Op-Amps A_1 and A_2 can be set at the same time adjusting just R_G.

For an exhaustive documentation on instrumentation amplifiers consult [2].



(a) *(b)*

Figure 4.3: Improved input stages of the basic instrumentation amplifier.

4.1.3 Voltage to Current Converter (Transconductance Amplifier)

A voltage to current converter is an amplifier that produces a current proportional to the input voltage. The constant of proportionality is usually called *transconductance*. Figure 4.4 shows a Transconductance Op-Amp, which is nothing but a non inverting Op-Amp scheme.

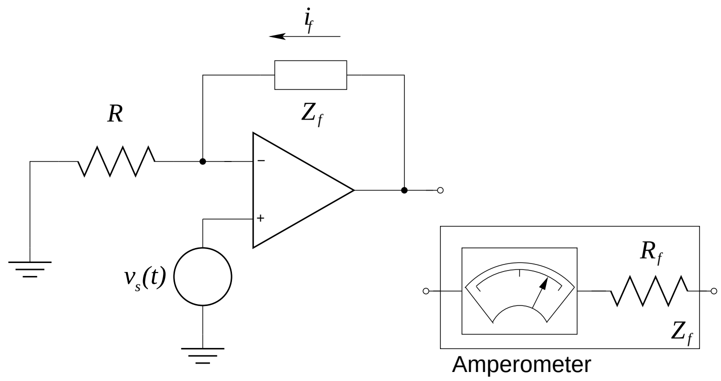


Figure 4.4: Basic transconductance amplifier circuit.

The current flowing through the impedance Z_f is proportional to the voltage v_s. In fact, supposing the infinite input impedance of the Op-Amp, we will have

$$i_f(t) = \frac{v_s(t)}{R}.$$

Placing an amperometer in series with a resistor with large resistance as a feedback impedance, we will have a high resistance voltmeter. In other words, the induced perturbation of such circuit will be very small because of the very high impedance of the operational amplifier.

4.1.4 Current to Voltage Converter (Transresistance Amplifier)

A current to voltage converter is an amplifier that produces a voltage proportional to the input current. The constant of proportionality is called *transimpedance* or *transresistance*, and its units are Ω. Figure 4.5 show a basic configuration for a transimpedance Op-Amp. Due to the virtual ground the current through the shunt resistance is zero, thus the output voltage is the voltage difference across the feedback resistor R_f, i.e.

$$v_o(t) = -R_f\, i_s(t).$$

Photo-multipliers photo-tubes and photodiodes drivers are a typical application for transresistance Op-amps. In fact, quite often the photo-current produced by those devices need to be amplified and converted into a voltage before being further manipulated.

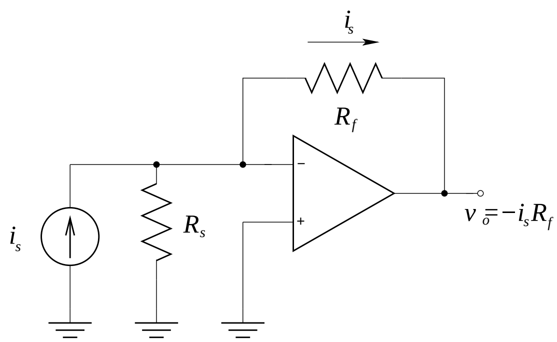


Figure 4.5: Basic transimpedance Op-Amp.

4.2 Logarithmic Circuits

By combining summing circuits with logarithmic and anti-logarithmic amplifiers we can build analog multipliers and dividers. The circuits presented here implements those non-linear operations just using the exponential current response of the semiconductor junctions. Because of that, they lack on temperature stability and accuracy. In fact, the diode reverse saturation current introduces an offset at the circuits output producing a systematic error. The temperature dependence of the diode exponential response makes the circuit gain to drift with the temperature. Nevertheless these circuits have a pedagogical interest and are the basis for more sophisticated solutions. For improved logarithmic circuits consult [1] chapter 7, and [1] section 16-13 and[3].

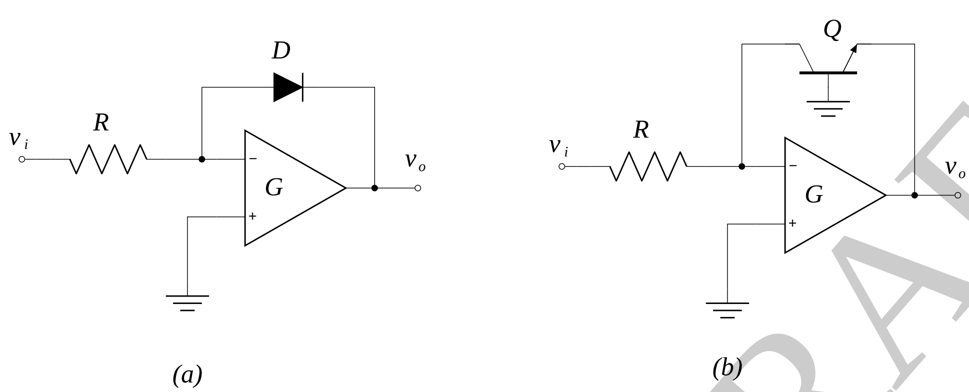


Figure 4.6: Elementary logarithmic amplifiers using a diode or an npn BJT.

4.2.1 Logarithmic Amplifier

Figure 4.6 (a) shows an elementary logarithmic amplifier implementation whose output is proportional to the logarithm of the input. Let's analyze this non-linear amplifier in more detail.

The Op-Amp is mounted as an inverting amplifier, and therefore if v_i is positive, then v_o must be negative and the diode is in conduction. The diode characteristics is

$$i = I_s \left(e^{-qv_o/k_B T} - 1 \right) \simeq I_s e^{-qv_o/k_B T} \qquad I_s \ll 1,$$

where $q < 0$ is the electron charge. Considering that

$$i = \frac{v_i}{R},$$

after some algebra we finally get

$$v_o = \frac{k_B T}{-q} \left[\ln(v_i) - \ln(RI_s) \right] .$$

The constant term $\ln(RI_s)$ is a systematic error that can be measured and subtracted at the output. It is worth to notice that v_i must be positive to have the circuit working properly. An easy way to check the circuit is to send a triangular wave to the input and plot v_o versus v_i. Because the BJT collector current I_c versus V_{BE} is also an exponential curve, we can replace the diode with an npn BJT as shown in Figure 4.6. The advantage of using a transistor as feedback path is that it should provide a larger input dynamic range.

If the circuit with the BJT oscillates at high frequency, a small capacitor in parallel to the transistor should stop the oscillation.

4.2.2 Anti-Logarithmic Amplifier

Figure 4.7 (a) shows an elementary anti-logarithmic amplifier, i.e. the output is proportional to the inverse of logarithm of the input. The current flowing through the diode is

$$i \simeq I_s e^{-qv_i/k_B T} \qquad I_s \ll 1.$$

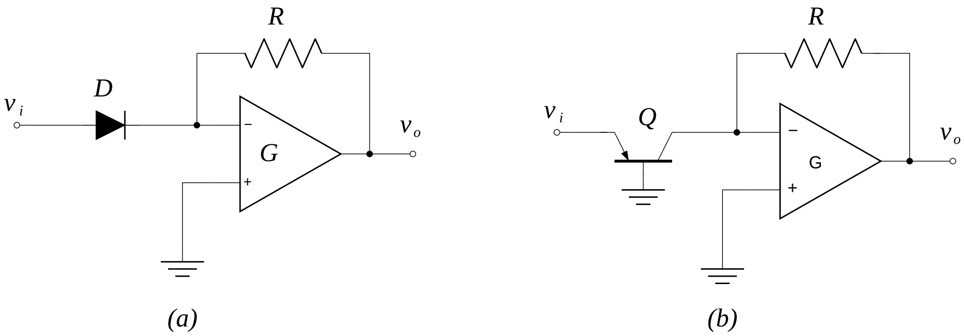


Figure 4.7: Elementary anti-logarithmic amplifiers using a diode or an pnp BJT.

Considering that

$$v_o = -Ri\,,$$

thus

$$v_o \simeq -RI_s e^{-qv_i/k_BT}.$$

If the input v_i is negative, we have to reverse the diode's connection. In case of the circuit of Figure 4.7 (b) we need to replace the pnp BJT with an npn BJT. Same remarks of the logarithmic amplifier about the BJT, applies to this circuit.

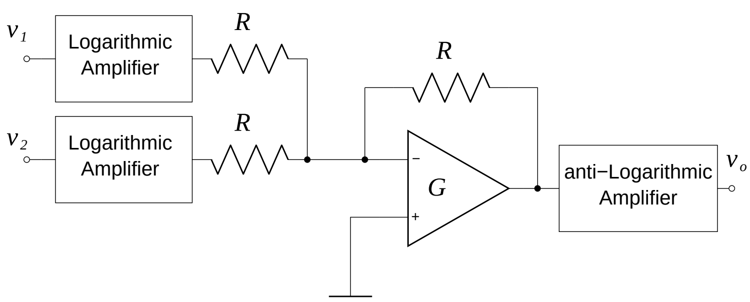


Figure 4.8: Elementary analog multiplier implementation using logarithmic and anti-logarithmic amplifiers

4.2.3 Analog Multiplier

Figure 4.8 shows an elementary analog multiplier based on a two log one anti-log and one adder circuits. Fore more details about the circuit see [1] section 7-4 and [1] section 16-13.

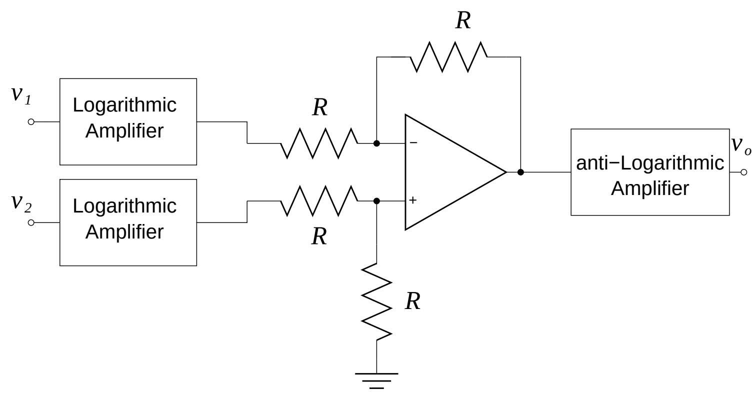


Figure 4.9: Elementary analog divider implementation using logarithmic and anti-logarithmic amplifiers.

4.2.4 Analog Divider

Figure 4.8 shows an elementary logarithmic amplifier based on a two log one anti-log and one adder circuits. Fore more details about the circuit see [1] section 7-5 and [1] section 16-13.

4.3 Multiple-Feedback Band-Pass Filter

Figure 4.10 shows the so called multiple-feedback bandpass, a quite good scheme for large pass-band filters, i.e. moderate quality factors around 10.

Here is the recipe to get it working. Select the following parameter which define the filter characteristics, i.e the center angular frequency ω_0 the quality factor Q or the the pass-band interval (ω_1, ω_2) , and the pass-band gain A_{pb}

$$\begin{aligned}\omega_0 &= \sqrt{\omega_2\omega_1} \\ Q &= \frac{\omega_0}{\omega_2 - \omega_1} \\ A_{pb} &< 2Q^2\end{aligned}$$

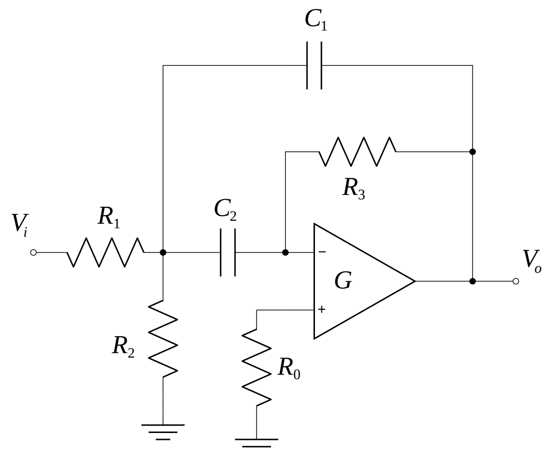


Figure 4.10: Multiple-feedback band-pass filter.

Set the same value C for the two capacitors and compute the resistance values

$$
\begin{aligned}
R_1 &= \frac{Q}{\omega_0 C A_{pb}} \\
R_2 &= \frac{Q}{\omega_0 C\left(2Q^2 - A_{pb}\right)} \\
R_3 &= \frac{2Q}{\omega_0 C}
\end{aligned}
$$

Verify that

$$A_{pb} = \frac{R_3}{2R_1} < 2Q^2$$

See [1] sections 8-4.2, and 8-5.3 for more details.

4.4 Peak and Peak-to-Peak Detectors

The peak detector circuit is shown in Figure 4.11. The basic ideal is to implement an integrator circuit with a memory.

To understand the circuit letŽs first short circuit D_0 and remove R. Then the Op-amp A_0 is just a unitary gain voltage follower that charges the capacitor C up to the peak voltage. The function of D_0 and of A_1 (high input impedance) is to prevent the fast discharge of the capacitor.

Because of D_0 the voltage across the capacitor is not the max voltage at the input, and this will create a systematic error at the output v_o. Placing a feedback from v_o to v_i will fix the problem. In fact, because v_+ must be equal to v_-, A_0 will compensate for the difference.

Introducing the resistance ($R \simeq 100\text{k}\Omega$) in the feedback will provide some isolation for v_o when v_i is lower than v_C.

The Op-Amp A_0 should have a high slew rate (~20 V/µs) to avoid the maximum voltage being limited by the Op-Amp slew rate.

The capacitor doesn't have to limit the Op-Amp A_0 slew rate S, i. e.

$$\frac{i_C}{C} \ll \frac{dv}{dt} = S$$

It is worthwhile to notice that if D_0 and D_1 are reversed the circuit becomes a negative peak detector.

The technology of the hold capacitor C is important in this application. The best choice to reduce leakage is probably polypropylene, and after that polystyrene or Mylar.

Using a positive and a negative peak detector as the input of a differential amplifier stage we can build a peak-to-peak detector (for more details see [1] section 9-1). Some things to check: holding time (a given % drop from the maximum) versus capacitor technology, systematic errors , settling time required for the output to stabilize.

4.5 Zero Crossing Detector

When v_i is positive and because it is connected to the negative input then v_o becomes negative and the diode $D_1$is forward biased and conducting.

4.6 Analog Comparator

An *analog comparator* or simply *comparator* is a circuit with two inputs v_i, v_{ref} and one output $v_o$which fulfills the following characteristic:

$$v_o = \begin{cases} V_1 & , v_i > v_{ref} \\ V_2, & v_i \leq v_{ref} \end{cases}$$

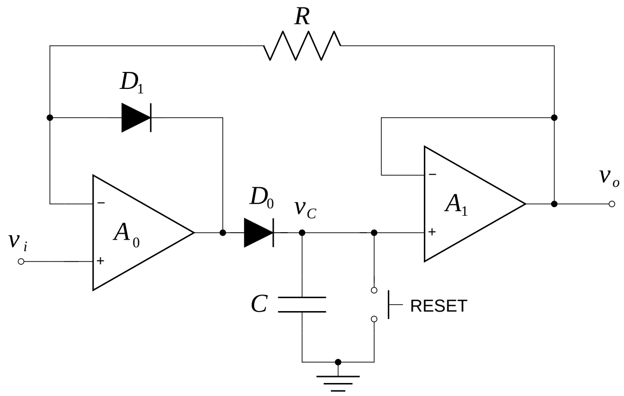


Figure 4.11: Peak detector circuit.

An Op-Amp with no feedback behaves like a comparator. In fact, if we apply a voltage $v_i > v_{ref}$, then $V_+ - V_- = v_i - v_{ref} > 0$. Because of the high gain, the Op-Amp will set v_o to its maximum value $+V_{sat}$which is a value close to the positive voltage of the power supply. If $v_i < v_{ref}$, then $v_o = -V_{sat}$. The magnitude of the saturation voltage are typically about 1V less than the supplies voltages.

Depending on which input we use as voltage reference v_{ref}, the Op-amp can be an inverting or a non inverting analog comparator.

4.7 Regenerative Comparator (The Schmitt Trigger)

The *Regenerative comparator* or *Schmitt Trigger*[1] shown in Figure 4.12 is a comparator circuit with hysteresis.

It is important to notice that the circuit has a positive feedback. With positive feedback, the gain becomes larger than the open loop gain making the comparator to swing faster to one of the saturation levels.

Considering the current flowing through R_1 and R_2,we have

[1]Otto Herbert Schmitt (1913-1998) American scientist considered the inventor of this device, that appeared in an article in 1938 with the name of "thermionic trigger"[**?**].

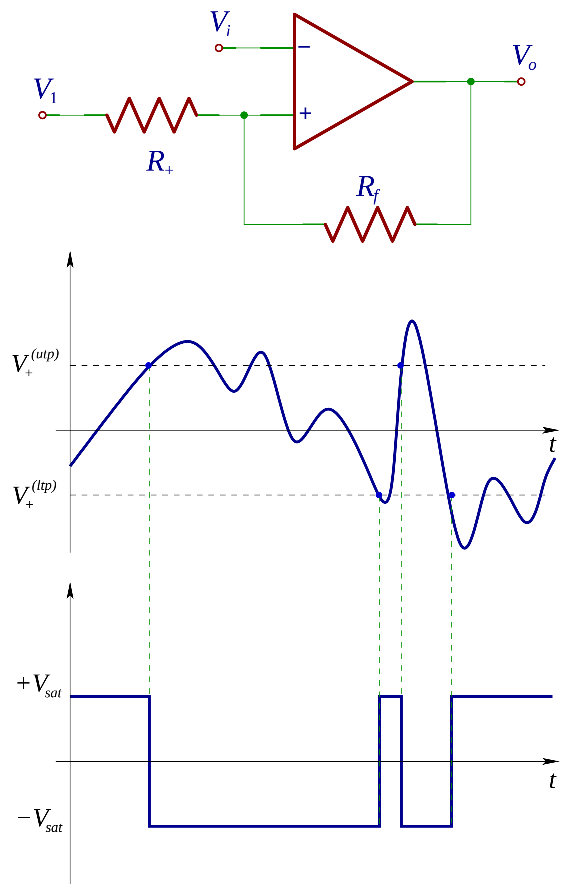


Figure 4.12: Schmitt Trigger and its qualitative response to a signal tha swings up and down between and through the saturation voltages $\pm V_{sat}$.

$$I = \frac{V_1 - V_+}{R_+} = \frac{V_+ - V_o}{R_f}, \qquad \Rightarrow \qquad V_+ = \frac{V_1 R_f + V_o R_+}{R_f + R_+}.$$

The output V_o can have two values, $\pm V_{sat}$. Consequently, V_+ will assume just two trip points values

$$V_+^{(utp)} = \frac{V_1 R_f + V_{sat} R_+}{R_f + R_+} \qquad V_+^{(ltp)} = \frac{V_1 R_f - V_{sat} R_+}{R_f + R_+}$$

When $V_i < V_+^{(utp)}$, V_o is high, and when $V_i < V_+^{(ltp)}$, V_o is low.

To set $V_+ = 0$ it requires that

$$V_1 = -\frac{R_+}{R_f} V_o$$

This circuit is usually used to drive an analog to digital converter (ADC). In fact, jittering of the input signal due to noise which prevents from keeping the output constant, will be eliminated by the hysteresis of the Schmitt trigger (values between the trip points will not affect the output).

See [1] section 11 for more detailed explanations.

Example1: ($V_{sat} = 15$V)

Supposing we want to have the trip points to be $V_+ = \pm 1.5V$, if we set $V_1 = 0$ then $R_f = 9R_+$.

4.8 Phase Shifter

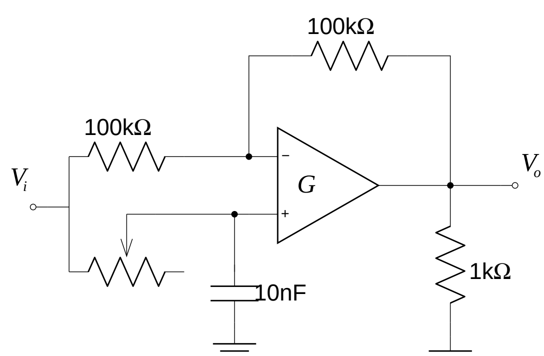


Figure 4.13: Phase shifter circuit.

A phase shifter circuit shown in Figure 4.13, produces a signal at the output V_0 which is equal to the input V_i with a phase shift φ given by the following formula

$$\tan\left(\frac{|\varphi|}{2}\right) = \frac{1}{RC\omega}$$

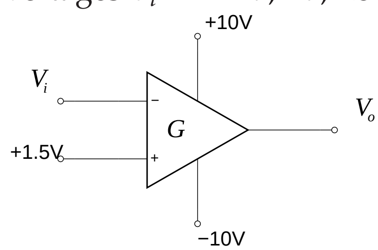
Supposing that we want a phase shift of $90^o$for a 1kHz sinusoid , then

$$R = \frac{1}{\tan\left(\frac{\varphi}{2}\right) C\omega} = \frac{1}{1 \cdot 10^{-8} \cdot 2\pi \cdot 10^{3}} = 15.915\text{k}\Omega.$$

Exchanging the potentiometer and the capacitor changes lead to lag.

4.9 Problems Preparatory to the Laboratory

1. Considering the following circuit, determine the voltage output V_o for the following input voltages $V_i = -2\text{V}, 1\text{V}, 1.5\text{V}, 3\text{V}$



2. Consider the Schmitt trigger of Figure 4.12.

   (a) If $V_o = -15\text{V}$ and $V_+ = 0\text{V}$, compute V_1.

   (b) If $V_o = +15\text{V}$, and $V_1 = 15\text{V}$, compute V_+.

3. Design a Schmitt trigger with two diode clamps and one resistor connected to the output.

   (a) Limit the output V_o from 0 to 5V.

   (b) Compute the resistance value R necessary to limit the diode current to 10mA.

4. What is the practical maximum and minimum output voltage of the logarithmic amplifier in Figure 4.6?

5. Chose and study at least two circuit to study and design. New circuits different than those ones proposed in this chapter are also welcome. For a good source of new circuits based on Op-Amps see [1] , [4], and [2].

4.10 Laboratory Procedure

No special procedure is required for this laboratory week. The student is encouraged to study, build and test more than one circuit (two at least) from this chapter and the next chapter on active filters. It is important also to try to find out circuit limitations, and to measure their performance.

Students are also encouraged to try basic Op-Amp applications different from the ones suggested in this notes.

Depending on the type of circuit the usual following measurements can be done to characterize the circuit

- Frequency response
- transient response
- Circuit output variation versus circuit parameter variation (voltage, resitance capacitance, etc..)

As usual, a report of the work done during the laboratory hours is required.

- Consult the data-sheets to properly connect the devices pin-out.
- Before powering your circuit up, always cross-check the power supply connections.
- It is always a good practice to turn on the dual power supply at the same time to avoid potential damages of electronic components.

Bibliography

[1] Luces M. Faulkenberry. An introduction to Operational Amplifiers with Linear IC Applications, Second Edition.

[2] Charles Kitchin and Lew Counts, A Designer's Guide to Instrumentation Amplifiers (2nd Edition), Analog Devices (http://www.analog.com/en/DCcList/0,3090,759%255F%255F42,00.html)

[3] Theory and Applications of Logarithmic Amplifiers, National Semiconductors, AN-311 (http://www.national.com/an/AN/AN-311.pdf).

[4] Horowitz and Hill, The Art of Electronics, Second Edition

[5] Microelectronics Jacob Millman & Arvin Grabel, McGraw-Hill Electrical Engineering Series

[6] A thermionic trigger, Otto H Schmitt 1938 J. Sci. Instrum. 15 24-26.

Chapter 5

Active Filters

Introduction

An electronic circuit that modifies the frequency spectrum of an arbitrary signal is called filter. A filter that modifies the spectrum producing amplification is said to be an active filter. Vis-à-vis its definition, it is convenient to study the filter characteristics in terms of the frequency response of its associated two port network

$$H(\omega) = \frac{V_o(\omega)}{V_i(\omega)} \ ,$$

where V_i and V_o are respectively the input voltage and the output voltage of the network, and ω the angular frequency. Depending on the design, active filters have some important advantages:

- they can provide gain,
- they provide isolation because of the typical impedance characteristics of amplifiers,
- they can be cascaded because of the typical impedance characteristics of amplifiers,
- they can avoid the use of inductors greatly simplifying the design of the filters.

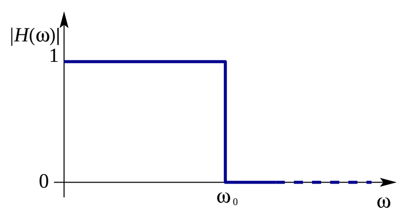
Here some disadvantages:

- they are limited by the amplifiers' band-with and noise,
- they need power supplies,
- they dissipate more heat.

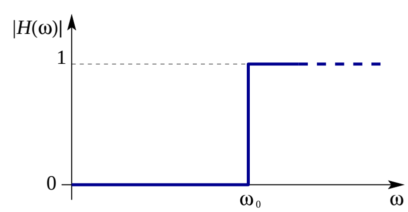
Let's make some simple definitions useful to classify different types of filters.

5.1 Classification of Ideal Filters

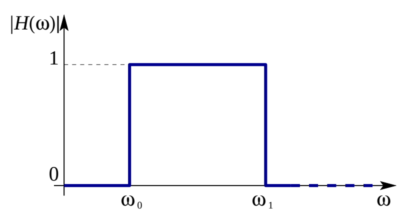
Based on their magnitude response $|H(\omega)|$, Some basic ideal filters can be classified as follows:



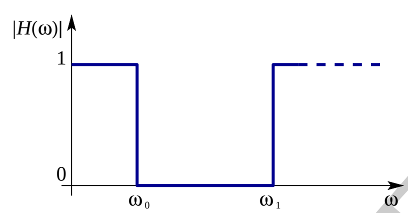
Low-pass



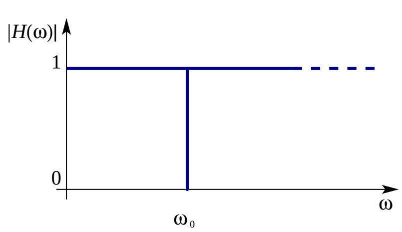
High-pass



Band-pass



Stop-band/band-reject



Notch

Practical filters approximate more or less the ideal definitions.

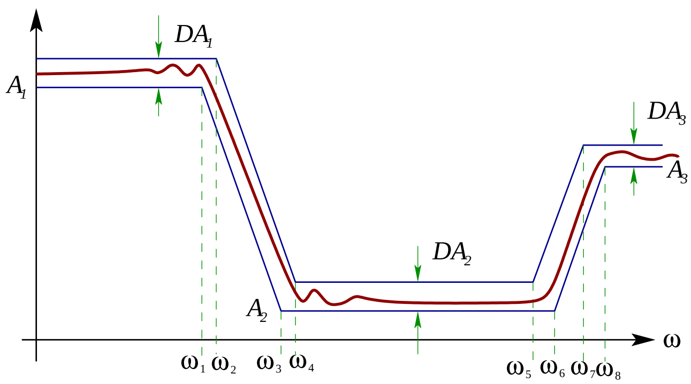


Figure 5.1: Graphical definition of the filter performance specifications, and hypothetical filter response (red curve) that satisfy the specification.

Usually, the filter requirements are specified defining the band frequencies with their gains (attenuation or amplification) gain ripples, and slope transitions in terms of power of the frequency. Figure 5.1 shows a quite general graphical definition of the design parameters of a filter with an hypothetical design. For a complete specification one should also define the requirement for phase response.

5.2 Filters as Rational Functions

Let's consider filters whose transfer function can be expressed as rational function or standard form

$$H(\omega) = \frac{\alpha_0 + \alpha_1 j\omega + \alpha_2 (j\omega)^2 + \ldots + \alpha_N (j\omega)^N}{\beta_0 + \beta_1 j\omega + \beta_2 (j\omega)^2 + \ldots + \beta_M (j\omega)^M}.$$

For the filter not to diverge

$$M \geq N \qquad \Rightarrow \qquad |H(\omega)| < \infty \text{ for any value of } \omega$$

Writing the transfer function as a polynomial factorization we obtain

$$H(\omega) = k\frac{(\omega - z_1)^{n_1} (\omega - z_2)^{n_2} \ldots (\omega - z_N)^{n_N}}{(\omega - p_1)^{m_1} (\omega - p_2)^{m_2} \ldots (\omega - p_M)^{m_M}}$$

Denominator roots $p_1, p_2, \ldots, p_n$ are called poles, and numerator roots $z_1, z_2, \ldots, z_m$ are called zeros. The integers $n_1, n_{2,} \ldots, n_N$, and $m_1, m_{2,} \ldots, m_N$ are therefore the multiplicity of poles and zeros.

Poles and zeros values determine the shape of the filter, and one could say that poles provides attenuation and zeros amplification.

The transition from transmission to attenuation and vice versa in the filter magnitude $|H(\omega)|$ is characterized by an asymptote slope which determine the so called filter order.

For example, considering the RC low pass filter with $\omega_0 = 1/RC$, we have one pole $p_1 = j\omega_0$

$$H(\omega) = \frac{\omega_0}{\omega_0 + j\omega} \Rightarrow \text{ first oder low pass filter with cut-off freq. } \omega_0$$

For example, considering the RC high pass filter with $\omega_0 = 1/RC$, we have one pole $p_1 = j\omega_0$ and one zero $z_1 = 0$

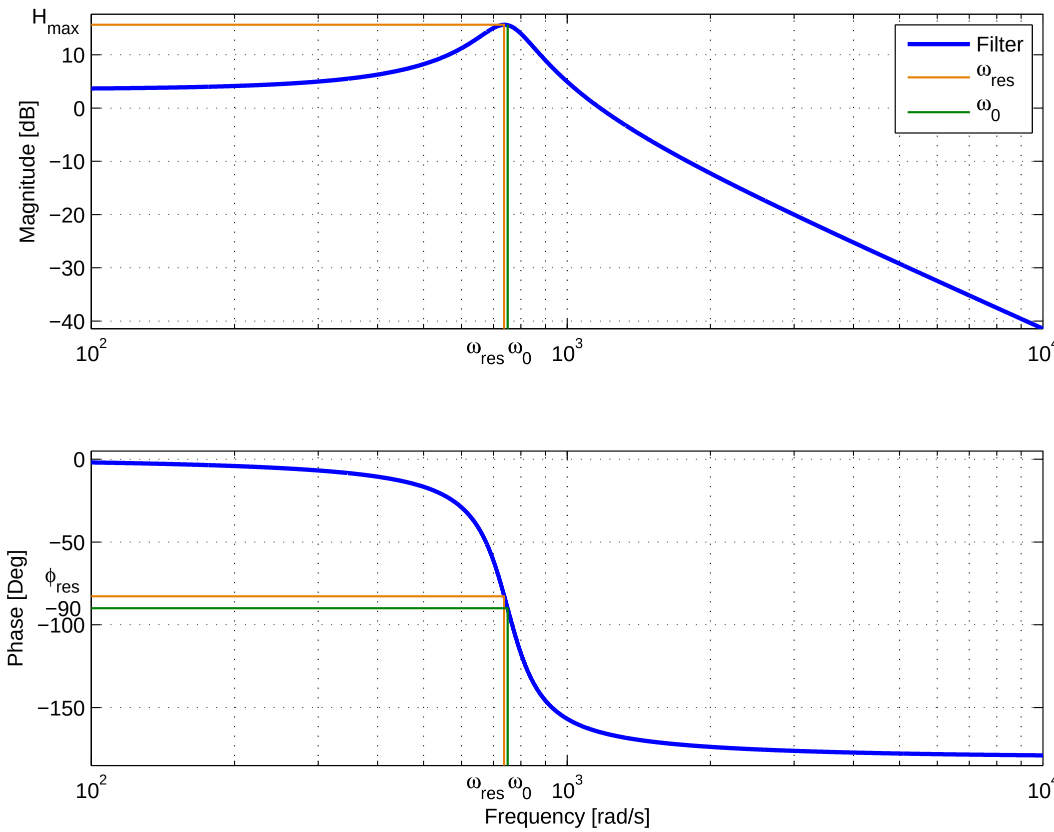
$$H(\omega) = \frac{\omega}{\omega_0 + j\omega} \Rightarrow \text{ first oder high pass filter with cut-off freq. } \omega_0$$

We will analyze into more detail filters with the following transfer function

$$H(\omega) = H_0 \frac{\omega^2 + j\omega a_1 + a_0}{-\omega^2 + j\omega\frac{\omega_0}{Q} + \omega_0^2}$$

5.2.1 Second Order Low-Pass Filter

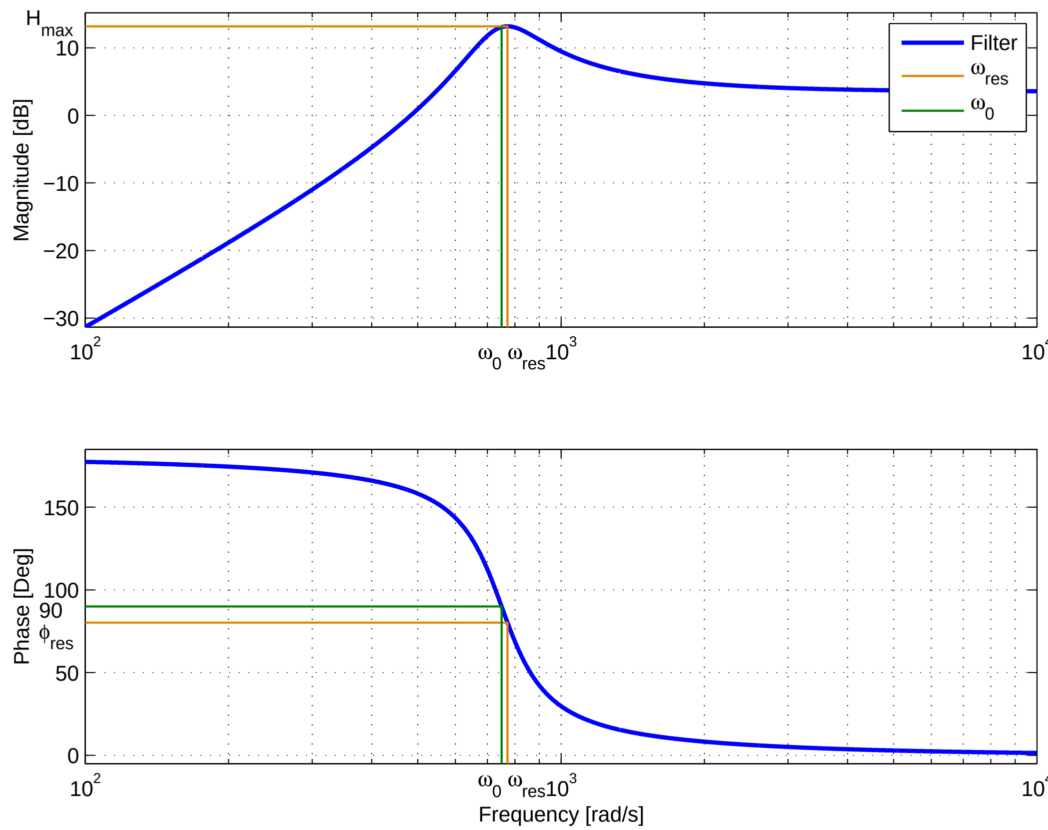
Figure below shows the second order low pass filter bode plot, with resonant frequency ω_{res}, and characteristic frequency ω_0



The second order low-pass filter written in standard form

Transfer Function	Resonance	Maximum	DC Gain	High Freq. Gain
$H_0 \dfrac{\omega_0^2}{-\omega^2 + j\omega\dfrac{\omega_0}{Q} + \omega_0^2}$	$\omega_0\sqrt{1-\dfrac{1}{2Q^2}}$	$H_0\dfrac{Q}{\sqrt{1-\dfrac{1}{4Q^2}}}$	H_0	0

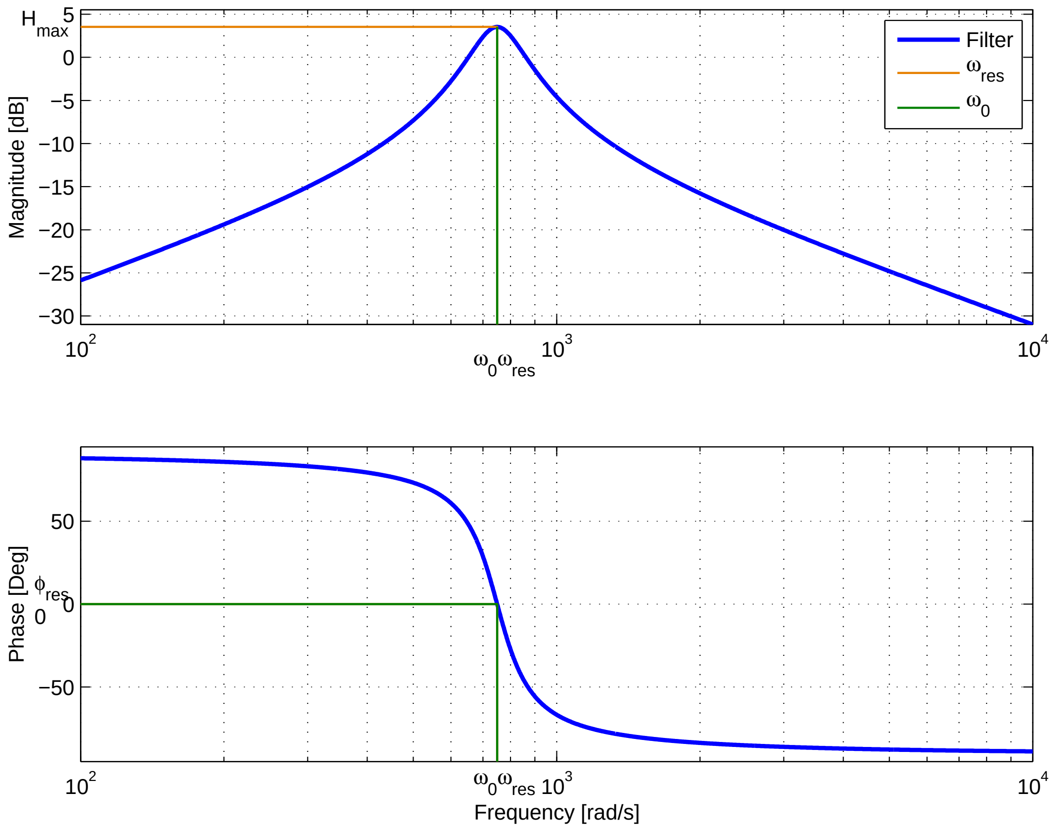
5.2.2 Second Order High-Pass Filter



The second order high-pass filter written in standard form

Transfer Function	Resonance	Maximum	DC Gain	High Freq. Gain
$H_0 \dfrac{\omega^2}{-\omega^2 + j\omega\dfrac{\omega_0}{Q} + \omega_0^2}$	$\dfrac{\omega_0}{\sqrt{1 - \dfrac{1}{2Q^2}}}$	$H_0 \dfrac{Q}{\sqrt{1 - \dfrac{1}{4Q}}}$	0	H_0

5.2.3 Band-Pass Filter



The band-pass filter written in standard form is

Transfer Function	Resonance	Maximum	DC Gain	High Freq. Gain
$H_0 \dfrac{j\omega\frac{\omega_0}{Q}}{-\omega^2 + j\omega\frac{\omega_0}{Q} + \omega_0^2}$	ω_0	H_0	0	0

For example, depending on the output we consider, the already studied LCR series circuit is a low-pass, a band-pass, or a high-pass filter with the transfer function described above. When we will study difference filters topologies we will reduce their transfer function into one of the standard form above.

5.3 Common Circuit Filters Topologies

This is a brief and not exhaustive at all list of filter topologies that use resistors, capacitors, and operational amplifiers to implement the filters types described above:

- Infinite gain, multiple feedback (IGMF). The name derives from the infinite gain of the active ideal element and double feedback topology (more that one feedback mesh).
- Generalized Sallen-Key (GSK)
- State Variable (SV)
- Switched Capacitor Filters (SC)
- Filter based on Gyrators, which implements inductors with capacitors and active components.

Cascading these implementation allows to increase the filter order.

5.4 Infinite Gain Multiple Feedback Configuration (IGMF)

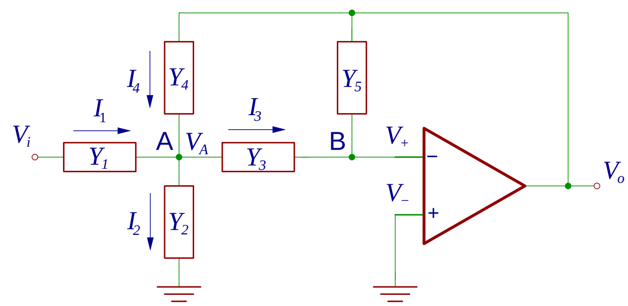


Figure 5.2: Infinite Gain Multiple Feedback Filter.

Let's consider the circuit in Figure 5.2 with generic admittances $Y_1, Y_2, Y_3, Y_4,$ and Y_5. Applying the KCL to node A and considering the circuit virtual ground $(V_- = 0)$, we have

$$V_A Y_3 + (V_o - V_A)\, Y_4 + (V_i - V_A)\, Y_1 + V_A Y_2 = 0\,. \tag{5.1}$$

Again, applying KCL to node B and for the virtual ground we have

$$V_o Y_5 + V_A Y_3 = 0 \quad \Rightarrow \quad V_A = -\frac{Y_5}{Y_3} V_o$$

Replacing the last expression into equation (5.1) and after some algebra we obtain the generic transfer function for the circuit

$$\frac{V_o}{V_i} = -\frac{Y_1 Y_3}{Y_5\,(Y_1 + Y_2 + Y_3 + Y_4) + Y_3 Y_4}\,.$$

Choosing the proper type of admittances we can construct different types of active filters, low-pass band-pass, and high-pass. It is worthwhile noticing that IGMF configuration allows to implement low-pass, band-pass, and high-pass filter with capacitors, resistor and no inductors. This simplifies considerably the design of the filters.

5.4.1 Low-pass Filter

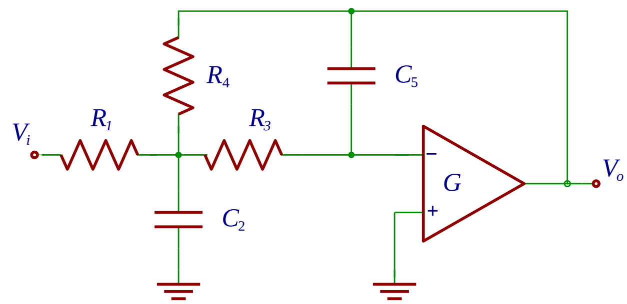


Figure 5.3: Low-pass filter configuration of the infinite gain multiple feedback filter.

A possible choice to implement a low-pass filter as shown in Figure 5.3 is

$$Y_1 = \frac{1}{R_1}, \qquad Y_2 = j\omega C_2, \qquad Y_3 = \frac{1}{R_3},$$

$$Y_4 = \frac{1}{R_4}, \qquad Y_5 = j\omega C_5,$$

and the transfer function of the circuit becomes

$$\frac{V_o}{V_i} = -\frac{{}^1\!/_{R_1R_3}}{j\omega C_5\left({}^1\!/_{R_1} + j\omega C_2 + {}^1\!/_{R_3} + {}^1\!/_{R_4}\right) + {}^1\!/_{R_3R_4}}.$$

Rearranging the expression to obtain a rational fraction in ω we finally obtain

$$\frac{V_o}{V_i} = \frac{-\dfrac{1}{R_1R_3C_2C_5}}{-\omega^2 + j\omega\dfrac{1}{C_2}\left({}^1\!/_{R_1} + {}^1\!/_{R_3} + {}^1\!/_{R_4}\right) + \dfrac{1}{R_3R_4C_2C_5}}.$$

Comparing the denominator of the previous equation with the denominator of the transfer function in section 5.2.1 we find that the frequency ω_0, the quality factor Q, and the DC gain H_0 are respectively

$$\omega_0 = \sqrt{\frac{1}{R_3R_4C_2C_5}}, \qquad Q = \omega_0\frac{C_2}{\left({}^1\!/_{R_1} + {}^1\!/_{R_3} + {}^1\!/_{R_4}\right)}, \qquad H_0 = -\frac{R_4}{R_1}.$$

5.4.2 High-pass Filter

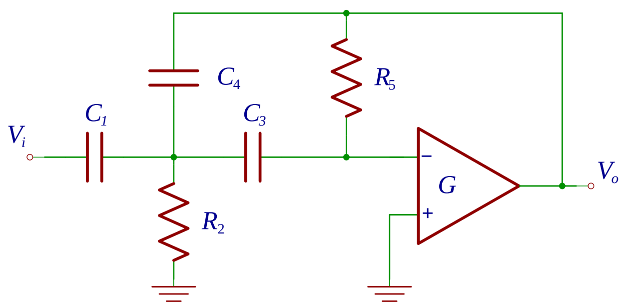


Figure 5.4: High-pass filter configuration of the infinite gain multiple feedback filter.

A possible choice to implement a high-pass filter as shown in Figure 5.4is

$$Y_1 = j\omega C_1, \qquad Y_2 = \frac{1}{R_2}, \qquad Y_3 = j\omega C_3,$$

$$Y_4 = j\omega C_4, \qquad Y_5 = \frac{1}{R_5},$$

and the transfer function of the circuit becomes

$$\frac{V_o}{V_i} = -\frac{j\omega C_1 j\omega C_3}{1/R_5\left(j\omega C_1 + 1/R_2 + j\omega C_3 + j\omega C_4\right) + j\omega C_3 j\omega C_4}.$$

Rearranging the expression to obtain a rational fraction in ω we obtain

$$\frac{V_o}{V_i} = \frac{-\omega^2\left(-C_1/C_4\right)}{-\omega^2 + j\omega\left(C_1 + C_3 + C_4\right)\frac{1}{R_5 C_3 C_4} + \frac{1}{R_2 R_5 C_3 C_4}}.$$

Comparing the denominator of the previous equation with the denominator of the transfer function in section 5.2.2 we find that the frequency ω_0, the quality factor Q, High frequency gain $H_\infty$are respectively

$$\omega_0 = \sqrt{\frac{1}{R_2 R_5 C_3 C_4}}, \qquad Q = \omega_0 \frac{R_5 C_3 C_4}{\left(C_1 + C_3 + C_4\right)}, \qquad H_\infty = -\frac{C_1}{C_4}.$$

5.4.3 Band-pass Filter

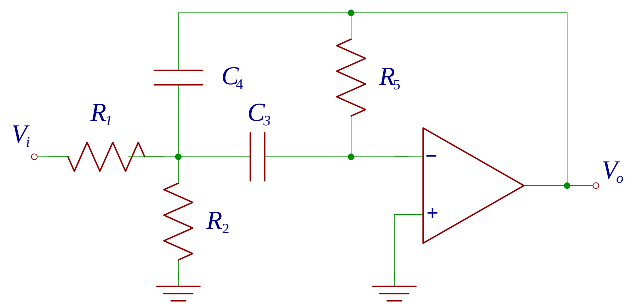


Figure 5.5: Band-pass filter configuration of the infinite gain multiple feedback filter.

A possible choice to implement a Band-pass filter is shown in Figure 5.5. The admittances are

$$Y_1 = \frac{1}{R_1}, \qquad Y_2 = \frac{1}{R_2}, \qquad Y_3 = j\omega C_3,$$

$$Y_4 = j\omega C_4, \qquad Y_5 = \frac{1}{R_5},$$

and the transfer function of the circuit becomes

$$\frac{V_o}{V_i} = -\frac{j\omega C_3/R_1}{{}^1/_{R_5}\left({}^1/_{R_1} + {}^1/_{R_2} + j\omega C_3 + j\omega C_4\right) + j\omega C_3 j\omega C_4}.$$

Rearranging the expression to get a rational fraction in ω we finally obtain

$$\frac{V_o}{V_i} = -C_1\frac{R_5}{R_1}\frac{j\omega\left(\dfrac{C_3+C_4}{R_5C_3C_4}\right)}{-\omega^2 + j\omega\dfrac{C_3+C_4}{C_3C_4R_5} + \dfrac{R_1+R_2}{R_1R_2R_5C_3C_4}}.$$

Comparing the denominator of the previous equation with the denominator of the transfer function in section 5.2.3 we find that the resonance frequency, and the quality factor are respectively

$$\omega_0 = \sqrt{\frac{R_1+R_2}{R_1R_2R_5C_3C_4}}, \qquad Q = \omega_0^2\frac{R_5C_3C_4}{C_3+C_4}, \qquad H_0 = -C_1\frac{R_5}{R_1}$$

5.5 Generalized Sallen-Key Filter Topology (GSK)

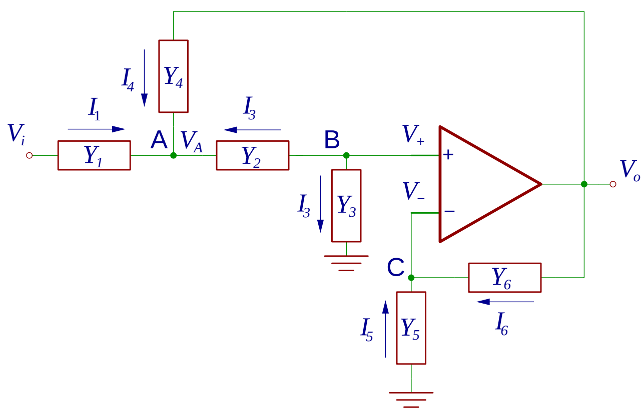


Figure 5.6: Generalized Sallen-Key Topology.

Let's consider the circuit in Figure 5.6 with generic admittances Y_1, Y_2, Y_3, Y_4, Y_5, and Y_6. Applying the KCL to node A , we have

$$(V_i - V_A)\,Y_1 + (V_o - V_A)\,Y_4 + (V_+ - V_A)\,Y_2 = 0\,. \tag{5.2}$$

Applying KCL to node B

$$(V_+ - V_A)\,Y_2 + V_+Y_3 = 0 \quad \Rightarrow \quad V_A = \frac{Y_2 + Y_3}{Y_2}V_+\,.$$

Applying KCL to node C

$$(V_0 - V_-)\,Y_6 - V_-Y_5 = 0 \quad \Rightarrow \quad V_- = V_+ = \frac{Y_6}{Y_6 + Y_5}V_0\,.$$

Replacing the expression found for V_A, and V_+ into equation (5.2) and after quite some boring algebra, we obtain

$$\frac{V_o}{V_i} = \left(1 + \frac{Y_5}{Y_6}\right)\frac{Y_1Y_2Y_6}{Y_1Y_6\,(Y_2 + Y_3) + Y_3Y_6\,(Y_2 + Y_4) - Y_2Y_4Y_5}\,.$$

Let's analyze some admittances' configuration of the this filter topology.

5.5.1 GSK Second Order Low-pass Filter

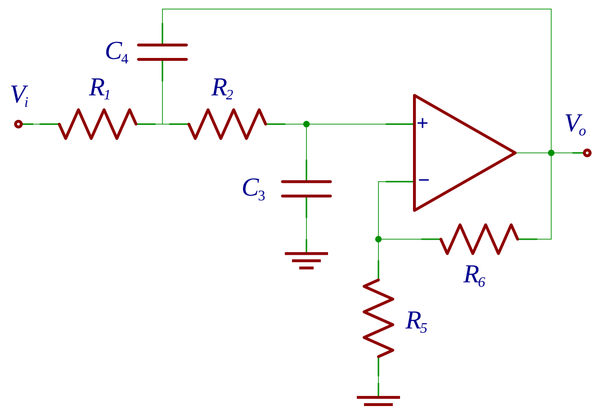


Figure 5.7: Low-pass filter configuration of the Generalized Sallen-Key filter.

A possible choice to implement a low-pass filter as shown in Figure 5.7 is

$$Y_1 = \frac{1}{R_1}, \qquad Y_2 = \frac{1}{R_2}, \qquad Y_3 = j\omega C_3,$$

$$Y_4 = j\omega C_4, \qquad Y_5 = \frac{1}{R_5}, \qquad Y_6 = \frac{1}{R_6},$$

and the transfer function of the circuit becomes

$$\frac{V_o}{V_i} = \left(1 + \frac{R_6}{R_5}\right) \frac{\frac{1}{R_1 R_2 C_3 C_4}}{-\omega^2 + j\omega\left(\frac{1}{R_1 C_4} + \frac{1}{R_2 C_4} - \frac{1}{R_2 C_3}\frac{R_6}{R_5}\right) + \frac{1}{R_1 R_2 C_3 C_4}}.$$

Comparing the denominator of the previous equation with the denominator of the transfer function in section 5.2.1we find that the frequency square ω_0^2, the quality factor Q, and the DC gain H_0 are respectively

$$\omega_0^2 = \frac{1}{R_1 C_4 R_2 C_3}, \qquad Q = \omega_0 \frac{R_1 R_2 R_5 C_3 C_4}{R_5 (R_1 + R_2) C_3 - R_1 R_6 C_4}, \qquad H_0 = \left(1 + \frac{R_6}{R_5}\right).$$

5.5.2 Simple Case

If $R_1 = R_2 = R$, $C_3 = C_4 = C$, and $R_5 = R_6 = 0$, then

$$\frac{V_o}{V_i} = \frac{\omega_0^2}{-\omega^2 + j\omega\omega_0 + \omega_0^2}, \qquad \omega_0^2 = \frac{1}{R^2C^2}, \qquad , Q = 1,$$

which is the transfer function of a second order low-pass filter with low quality factor.

5.5.3 GSK Second Order High-pass Filter

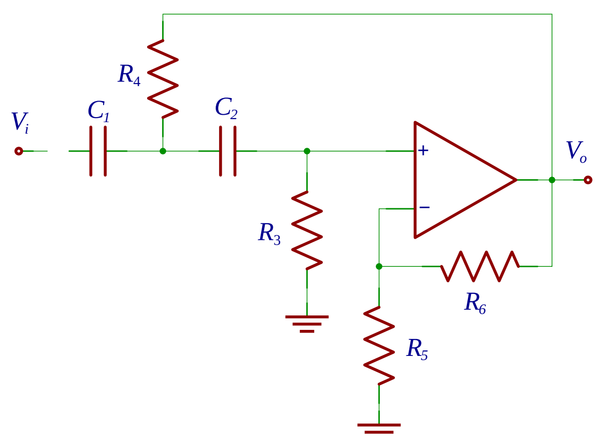


Figure 5.8: High-pass filter configuration of the Generalized Sallen-Key filter.

To implement a low-pass filter as shown in Figure 5.8 one needs to choose the admittances as follows

$$Y_1 = j\omega C_1, \qquad Y_2 = j\omega C_2, \qquad Y_3 = \frac{1}{R_3},$$

$$Y_4 = \frac{1}{R_4}, \qquad Y_5 = \frac{1}{R_5}, \qquad Y_6 = \frac{1}{R_6},$$

and the transfer function of the circuit becomes

$$\frac{V_o}{V_i} = \left(1+\frac{R_6}{R_5}\right)\frac{-\omega^2}{-\omega^2 + j\omega\left(\frac{1}{R_3C_2}+\frac{1}{R_3C_1}-\frac{1}{R_4C_1}\frac{R_6}{R_5}\right)+\frac{1}{R_3R_4C_1C_2}}.$$

Comparing the denominator of the previous equation with the denominator of the transfer function in section 5.2.2 we find that the frequency square ω_0^2, the quality factor Q, and the DC gain H_0 are respectively

$$\omega_0^2 = \frac{1}{R_3C_1R_4C_2}, \qquad Q = \omega_0 \frac{R_3R_4R_5C_1C_2}{R_5\left(C_1+C_2\right)R_3 - C_1R_6R_4}, \qquad H_0 = \left(1+\frac{R_6}{R_5}\right).$$

5.5.4 Simple Case

If $R_1 = R_2 = R$, $C_3 = C_4 = C$, and $R_5 = R_6 = 0$, then

$$\frac{V_o}{V_i} = \frac{-\omega^2}{-\omega^2 + j\omega\omega_0 + \omega_0^2}, \qquad \omega_0^2 = \frac{1}{R^2C^2}, \qquad , Q = 1,$$

which is the transfer function of a second order high-pass filter with low quality factor.

5.5.5 GSK Band-pass Filter

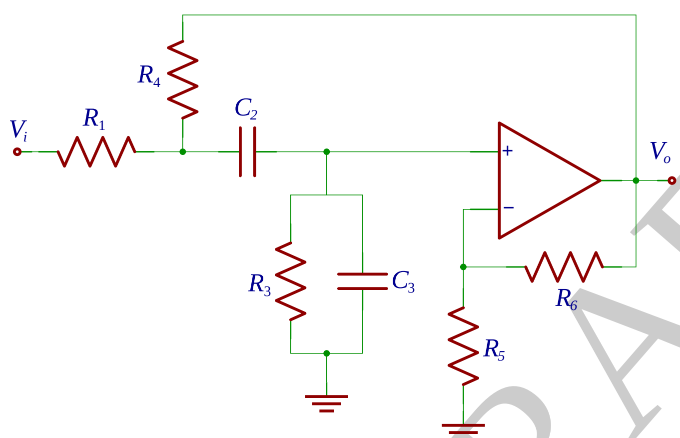


Figure 5.9: Band-pass filter configuration of the Generalized Sallen-Key filter.

To implement a band-pass filter as shown in Figure 5.9 one needs to choose the admittances as follows

$$Y_1 = \frac{1}{R_1}, \qquad Y_2 = j\omega C_2, \qquad Y_3 = \frac{1}{R_3} + j\omega C_3,$$
$$Y_4 = \frac{1}{R_4}, \qquad Y_5 = \frac{1}{R_5}, \qquad Y_6 = \frac{1}{R_6},$$

and the transfer function of the circuit becomes

$$\frac{V_o}{V_i} = \left(1 + \frac{R_6}{R_5}\right) \frac{\frac{j\omega}{R_1 C_3}}{-\omega^2 + j\omega\left(\frac{C_2 + C_3}{C_2 C_3 R_1} + \frac{1}{C_3 R_3} + \frac{1}{C_2 R_4} - \frac{1}{C_3 R_4}\frac{R_6}{R_5}\right) + \frac{R_1 + R_4}{C_2 C_3 R_1 R_3 R_4}}.$$

Comparing the denominator of the previous equation with the denominator of the transfer function in section 5.2.3 we find that the frequency square ω_0^2, the quality factor Q, and the DC gain H_0 are respectively

$$\omega_0^2 = \frac{R_1 + R_4}{C_2 C_3 R_1 R_3 R_4}, \qquad Q = \omega_0 \frac{C_2 C_3 R_1 R_3 R_4 R_5}{(C_2 + C_3) R_3 R_4 R_5 + C_2 R_1 R_4 R_5 + C_3 R_1 R_3 R_5 - C_2 R_1 R_3 R_6}, \qquad H_0 =$$

5.5.6 Simple Case

If $R_1 = R_3 = R_4 = R$, $C_2 = C_3 = C$, and $R_5 = R_6 = 0$, then

$$\frac{V_o}{V_i} = \frac{j\omega \frac{\omega_0}{Q}}{-\omega^2 + j\omega\frac{\omega_0}{Q} + \omega_0^2}, \qquad \omega_0^2 = \frac{2}{R^2 C^2}, \qquad , Q = \frac{\sqrt{2}}{3},$$

which is the transfer function of a second order high-pass filter with low quality factor.

5.6 State VariableFilter Topology (SV)

TBD

5.7 Practical Considerations

5.7.1 Component Values

How do we select the values of capacitance and resistance? Here are some considerations that should help the filter design:

- reducing the resistance values reduces the thermal noise and therefore the filter noise,
- reducing resistance values minimizes the op-amp voltage offsets,
- increasing the resistance reduce the current load on the op-amps,
- increasing the resistances usually allows to decrease the capacitance and therefore it make easier to find capacitors because of the small capacitance values needed,
- reducing the capacitance minimizes the capacitance fluctuations due to temperature,
- increasing the capacitance allows to reduce resistance values and therefore the thermal noise.

As we can clearly see, some of the consideration cannot be used at the same time. Based on the design requirements one can decide which of the consideration above are more important to finally meet the design requirements.

Rules of Thumb

Particularly critical design often overrule these following rules:

- Capacitor with capacitance less of ~100 pF should be avoided,
- Try to use resistor with resistance between few kilo-ohms to few hundreds of kilo-ohms.

5.7.2 Components technology

Capacitors

The use of low loss dielectric is very important to obtain good results. If possible one should use plastic film capacitors or C0G/NPO ceramic capacitors, 1% tolerance for temperature stability.

Resistor

Low thermal noise resistors such as metal film resistors 1% tolerance for temperature stability should be used.

Chapter 6

Basics on Oscillators

6.1 Introduction

Waveform generators are circuits which provide a periodic signal with constant frequency, phase, and amplitude. The quality of these devices are measured by the frequency stability, amplitude stability, and absence of distortion. The last characteristics is essentially cleanness of the spectrum signal. For example, the spectrum of a perfect sinusoidal oscillator must be a delta of Dirac at the oscillating frequency. Practically, sinusoidal oscillators has a sharp narrow peak at the oscillation frequency, and other less taller peaks at different frequencies, mainly at multiples of the oscillation frequency (harmonics).

In this chapter we will study the criterion to sustain a sinusoidal oscillation with a positive feedback amplifier, the so-called **Barkhausen criterion**, and some simple circuit to produce different waveforms.

Direct Digital Synthesis[1], a more versatile and effective technique to produce arbitrary waveforms, is out of the scope of these simple notes.

6.2 Barkhausen Criterion

Let's consider an ideal amplifier with a positive feedback network as show in figure 6.1. Considering that the summation point output is

$$V_i + \beta(\omega)V_o,$$

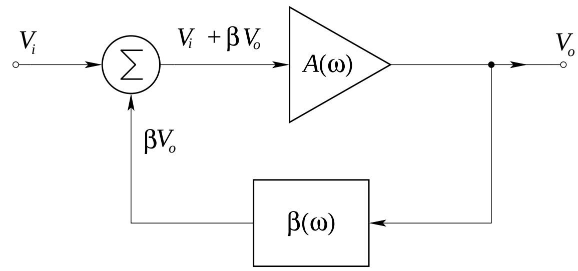


Figure 6.1: Amplifier with positive feedback

and the amplifier gain is $A(\omega)$, the output voltage will be

$$V_o = A(V_i + \beta V_o),$$

Collecting V_o we will finally have

$$V_o = \frac{A}{1 - \beta A} V_i.$$

For

$$|\beta(\omega)A(\omega)| = 1, \qquad \arg\left[\beta(\omega)A(\omega)\right] = 0, 360, ...$$

the output V_o diverges. If the previous condition is satisfied for the angular frequency ω_0, any excitation at the frequency ω_0 will make the output to oscillate at the frequency ω_0 with infinite amplitude. If $V_i$is equal to zero then the output will oscillate at the frequency ω_0 with the amplitude A.

The previous condition which can be rewritten as

$$\Re[\beta A] = 1, \qquad \Im[\beta A] = 0 \tag{6.1}$$

is the so called **Barkhausen criterion** for the oscillation.

The term βA is called the **open loop gain** or simply **loop gain** since that is exactly the gain of the loop in the feedback amplifier network when the loop is open at the summing point.

6.2.1 Practical Considerations

Oscillators with exactly unitary loop gain at a given frequency and input V_i equal to zero at any time are just a mere mathematical abstraction.

For example, external perturbations, drifts due to temperature, and aging would make this condition impossible to keep.

Practically, it is necessary to have a loop gain βA somewhat larger than unity to start and sustain the oscillation. This can lead to a slow drift of the oscillation amplitude, and in the worst case, the oscillation can even saturate or stop.

To properly sustain the oscillation in case of temperature drifts, we need to add to the positive feedback path another feedback loop this time negative to stabilize the gain. This path often called Automatic Control Circuit (AGC) can be done using temperature sensitive components. For example, semiconductor diodes or transistors whose resistivity decreases with the temperature can be used in the AGC.

It is worthwhile to notice that large values of the amplifier gain A produce saturation at the output, and therefore can be used to generate squares or pulse waves. Moreover, cascading a proper filtering stage, one can select just one frequency and make a quite amplitude stable sinusoidal generator.

We don't have to provide an initial kick to start the oscillation. This is true, because every time we switch a circuit on a step propagates through the circuit providing an initial excitation at the right frequency. Moreover, the probability to have a small signal fluctuation at the right frequency are usually quite high.

The frequency stability of the oscillator is a quite complex topic of study. Here we can simply say that it depends mainly on the ability of the circuit to maintain the loop gain phase constant to 0°or to multiples of 360°.

In the discussion of the oscillator circuits, we will assume that the amplifier is able to deliver the required positive or negative gain without adding any additional phase. In the general case, this is clearly a crude approximation, but it is used just to simplify the study of the circuits.

6.3 Phase Shift Oscillator

The phase shift oscillator exemplifies the concepts set forth above. Referring to figure 6.2, we can distinguish the JFET amplifier stage and the positive feedback network made of three cascaded RC phase shifting filters.

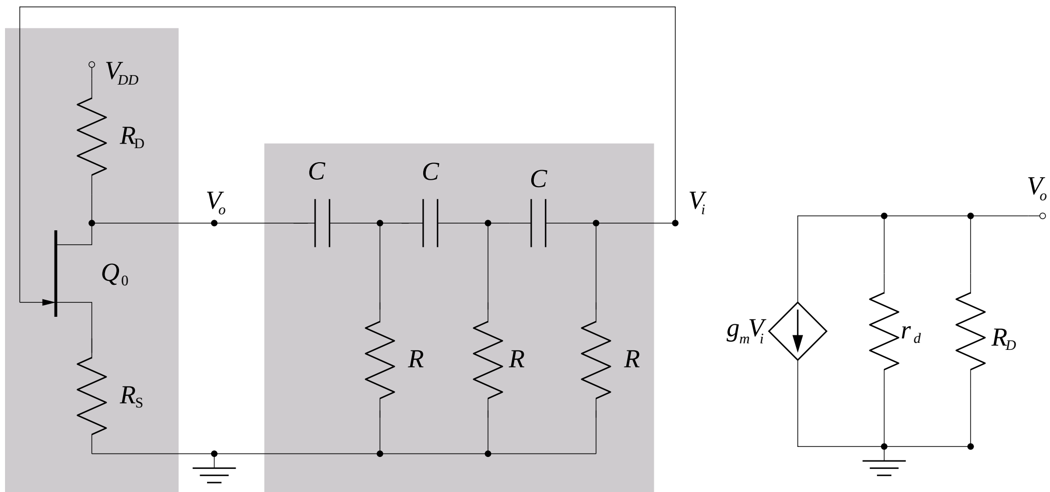


Figure 6.2: Phase shift oscillator using a JFET as amplification stage (left gray rectangle) and a phase shift network (right gray rectangle). The circuit on the left represents the low frequency model of the JFET amplifier.

Supposing that the amplifier load Z_L is negligible, i.e. $|Z_L| \gg R_D||r_d$ then, the amplifier will just change sign (180°) to any signal injected in the gate. The network feedback will provide additional phase shift to satisfy the Barkhausen criterion at a given angular frequency ω_0.

It can be proved that

$$\beta(\omega) = \frac{V_i}{V_o} = \frac{1}{1 - \frac{5}{(\omega\tau)^2} + j\left(\frac{1}{(\omega\tau)^3} - \frac{6}{\omega\tau}\right)} \qquad \tau = RC\,, \tag{6.2}$$

The amplifier gain, supposed to be constant is $A = -g_m R_D$, where g_m is the JFET amplifier gain.

Imposing the condition $\Im[\beta A] = 0$, we get

$$\omega_0 = \frac{1}{\sqrt{6}}\frac{1}{\tau}.$$

Replacing the previous expression in the open loop gain $A\beta$ and using the second condition $\Re\,[\beta A] = 1$, we get

$$g_m R_D = 29$$

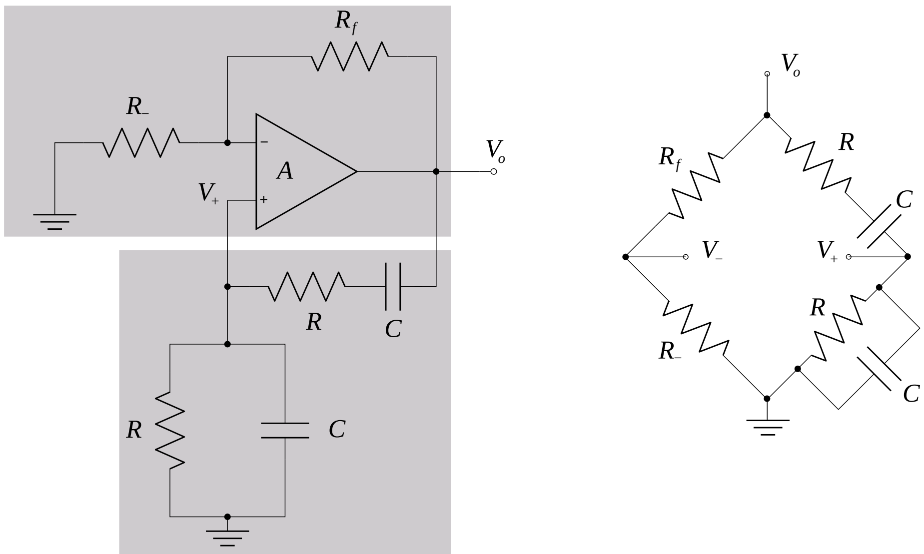


Figure 6.3: Wien bridge oscillator, and components rearrangement to show the bridge topology.

To sustain the oscillation, the amplifier must have a gain of at least $29/R_D$.

6.4 The Wien Bridge Oscillator

The Wien Bridge Oscillator show in figure 6.3, uses a differential amplifier to provide positive and negative feedback to satisfy the two condition of oscillation.

Referring to figure 6.3 , setting $Y_C = 1/\,(j\omega C)$, and thanks to the voltage divider equation we can write

$$V_+ = \frac{\frac{RY_C}{Y_C+R}}{R + Y_C + \frac{RY_C}{Y_C+R}} V_o = \frac{1}{\frac{(Y_C+R)^2}{RY_C} + 1} V_o = \frac{1}{\frac{Y_C}{R} + \frac{R}{Y_C} + 3} V_o$$

and

$$\beta(\omega) = \frac{V_+}{V_o} = \frac{1}{3 + j\left(\omega\tau - \frac{1}{\omega\tau}\right)} \qquad \tau = RC.$$

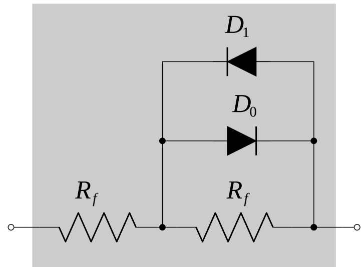


Figure 6.4: Automatic gain control circuit for the Wien bridge oscillator negative feedback.

The oscillation will happen where the phase shift is zero, i.e. for

$$\omega\tau - \frac{1}{\omega\tau} = 0, \qquad \Rightarrow \qquad \omega_0 = \frac{1}{\tau}\,.$$

The angular oscillation frequency ω_0 depends on the inverse of the resistance R and the capacitance C.

Because the attenuation at the resonant frequency is

$$\frac{V_+}{V_o} = \frac{1}{3}\,.$$

the negative feedback must have a theoretical gain of $A(\omega_0) = 3$. The resistances R_- and R_f must be given by the usual equation

$$\frac{V_{o'}}{V_+} = 1 + \frac{R_f}{R_-}\,.$$

The oscillation frequency can be continuously tuned using coupled variable resistors.

To minimize distortions due to the Op-amp saturation when the gain is larger than one, it is required to provide a circuit with variable gain. Essentially, we need an overall gain larger than one for small signal to sustain the oscillation and gain of about 1 or less for large signal to avoid distortion. The negative feedback path shown in figure 6.4 does the job. For large signals one of the diodes becomes forward biased reducing the feedback resistance and the Op-Amp gain. For smaller signal the gain is not affected by the diodes.

Practically, Wien Bridge oscillators are used in the kilohertz region with a variable range up to ~10 times ω_0.

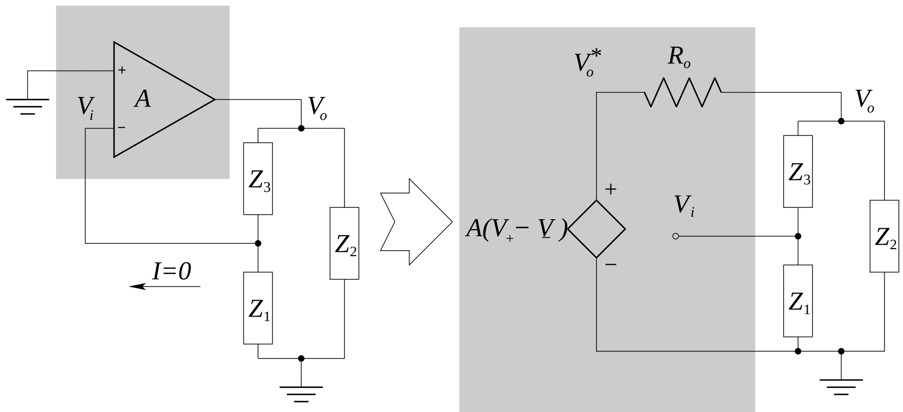


Figure 6.5: LC Oscillator circuit using an ideal Op-Amp with non zero output impedance R_o and its equivalent ideal circuit. Note that the feedback loop is connected to the negative input of the amplifier, and therefore to get a positive loop feedback the feedback network has to flip the signal phase by 180° .

6.5 LC Oscillator

A quite general form of oscillator circuits is depicted in figure 6.5. In this case it is not straightforward to separate the oscillating feedback network and the amplifier itself. Let's suppose that the amplifier is ideal but has a non zero output resistance R_o. Referring to figure 6.5 we have

$$\beta = \frac{V_i}{V_0^*}.$$

Applying the voltage divider equation twice we have the two equations

$$V_i = \frac{Z_1}{Z_1 + Z_3} V_o$$

and

$$V_o = \frac{Z}{Z + R_o} V_0^*, \qquad Z = Z_2 || \left(Z_1 + Z_3 \right) ,$$

or

$$\frac{1}{V_o^*} = \frac{Z}{Z + R_o} \frac{1}{V_0}.$$

After some algebra we finally get

$$\beta = \frac{Z_1 Z_2}{R_o\left(Z_1 + Z_2 + Z_3\right) + Z_2\left(Z_1 + Z_3\right)}\,. \tag{6.3}$$

Let's consider the case of the LC tunable oscillators, i.e. the impedances are purely reactive (real part equal to zero)

$$Z_i \;=\; jX_i\,, \qquad X_i > 0 \qquad \text{for } i = 1,2,3$$

Then the previous eq. (6.3) becomes

$$\beta = \frac{-X_1 X_2}{jR_o\left(X_1 + X_2 + X_3\right) - X_2\left(X_1 + X_3\right)}\,.$$

For β to be real

$$X_1 + X_2 + X_3 = 0\,,$$

and

$$\beta(\omega_0) = \frac{X_1}{X_1 + X_3}\,,$$

where ω_0 is the oscillation frequency. Using the two previous equation we finally get

$$\beta(\omega_0) = -\frac{X_1}{X_2} \qquad \Rightarrow A_{OL} = -A\left(-\frac{X_1}{X_2}\right).$$

Since A_{OL} must be positive and $A > 0$, then X_1 and X_2 must have same sign. For example they have be both capacitors or inductors. From the condition of imaginary part equal to zero we find that if X_1 and X_2 are capacitors, then X_3 must be an inductor, and vice versa. Here is the oscillator circuit name depending on the choice of the reactance:

- **Colpitts Oscillator**: X_1 and X_2 capacitive reactances and X_3 an inductive reactance ($X_{1,2} = -1/(\omega C_{1,2})$, $X_3 = \omega L_3$).
  The oscillator angular frequency and the gain in this case are

$$\omega_0 = \sqrt{\frac{1}{L_3\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}\,, \qquad \beta(\omega_0) = \frac{C_2}{C_1}$$

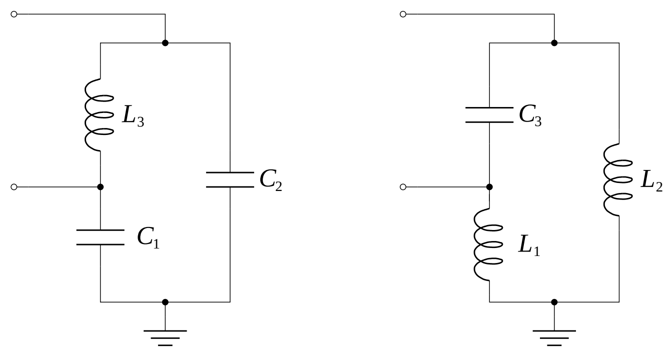


Figure 6.6: Colpitts (left) and Hartley (right) feedback circuits $\beta(\omega)$ for the LC oscillator circuit of Figure 6.5.

- **Hartley oscillator**: X_1 and X_2 inductive reactances and X_3 a capacitive reactance ($X_{1,2} = \omega L_{1,2}$, $X_3 = -1/(\omega C_3)$).
  The oscillator angular frequency and the gain in this case will be

$$\omega_0 = \sqrt{\frac{1}{C_3 \left(L_1 + L_2\right)}}, \qquad \beta(\omega_0) = \frac{L_1}{L_2}$$

Using a BJT amplifier we can usually obtain higher oscillating frequency than using standard operational amplifiers. In this case the high frequency hybrid-π model[2] must be used to properly model the transistor behavior. Moreover, the BJT amplifier low input impedance makes the design more complicated.

6.6 Crystal Oscillator

Crystal oscillators are based on the property of piezoelectricity[1] exhibited by some crystals and ceramic materials. Piezoelectric materials change size when an electric field is applied between two of its faces. Conversely, if we apply a mechanical stress, piezoelectric materials generate an electric field. Some crystals have internal mechanical resonances with very high

[1]Piezoelectricity was discovered by Jacques and Pierre Curie in the 1880's during experiments on quartz.

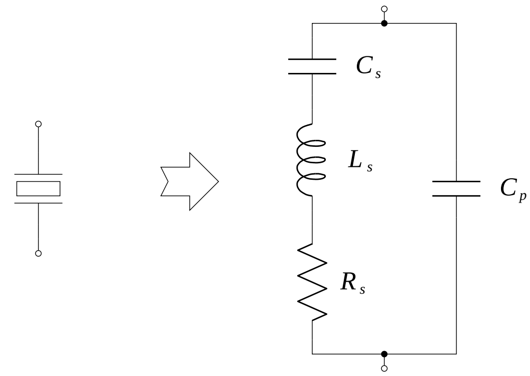


Figure 6.7: Circuit symbol for a piezoelectric oscillator (or quartz oscillator) and the equivalent electronic circuit. The LCR series circuit accounts for the sharp mechanical resonance The capacitor C_p in parallel describes the capacitance of the crystal for frequency far for the resonance.

quality factors (quartz can reach quality factors of 10^4) [2] and can be indeed used to generate very stable oscillators.

Figure 6.7 shows the circuit symbol for a piezoelectric component and the equivalent circuit modeled using ideal components.

Usually, to apply an electric field to a crystals is necessary to make a conductive coating on two parallel faces, and this process creates a capacitor with an interposed dielectric. This explain the presence of the capacitor of capacitance C_p in the model. The LCR series circuit accounts for the particular mechanical resonance we want to use to build the oscillator.

To design a crystal oscillator it is important to study the reactance (the imaginary part of the impedance) whose qualitative behavior is shown in figure 6.8. Where the reactance is essentially inductive and very close to the resonance, the crystal behaves as a simple equivalent inductor. We can indeed replace the inductor L_s of the LC oscillator of figure 6.5 with the piezoelectric crystal to build a simple oscillator.

Crystal oscillators using a Colpitts configuration and a BJT in common-emitter or common-collector configuration, can work from few kHz up to ~100MHz.

[2]Mechanical resonance stability depends mainly on the fact that the resonance value is determined by the crystal geometry. It the crystal size slightly depends on the temperature we can have very stable resonators. Active temperature stabilization can clearly improve frequency stability.

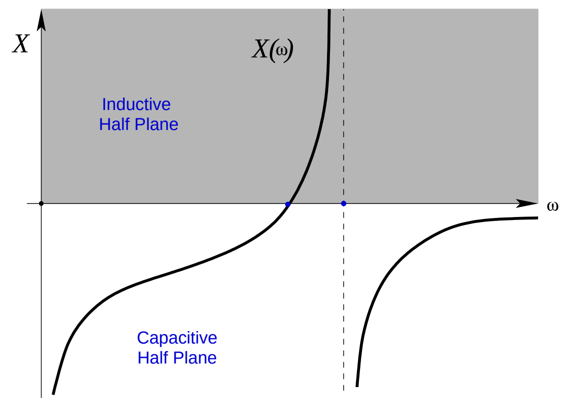


Figure 6.8: Qualitative behavior of the crystal reactance versus frequency.

6.7 Relaxation Oscillators

Relaxation oscillators include a wide class of non-linear systems, many of them in different fields such as mechanical, biological chemical, electrical fields to just mention a few.

Relaxation oscillators are characterized by the following properties:

- a non linear mechanism that provides a bistable state,
- a relaxation process that creates the transition from one stable state to the other,
- a period of oscillation characterized by a relaxation phenomena, i.e. by the time constant of the relaxation process,

The canonical example of relaxation oscillator is the seesaw with one bucket on one end and a weight on the other, with the bucket continuosly filled by a constant water flow. When the bucket is filled it changes the equilibrium of the seesaw and the system transitions to the new state. In the new state, the bucket is tilted enough to be emptied and therefore the system transition back to the older state. The seesaw + waterflow is clearly the bistable nonlinear system, and the relaxation process is the emptying of the bucket.

Vander Pol was one of the first to analize a relaxation oscillator system.

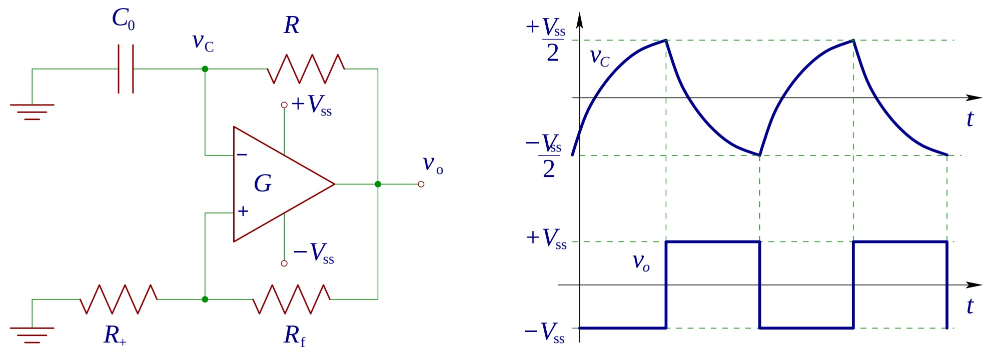


Figure 6.9: The Op-Amp version of the RC Charge Discharge Oscillator.

6.7.1 The RC Relaxation Oscillator

A very simple relaxation oscillator is the RC charge discharge oscillator show in figure 6.9. The ideal Op-Amp is configured as a Schmitt trigger which provides the non-linear bistable states. The negative feedback provides the relaxation mechanism.

To qualitatively understand the circuit, let's suppose that the Schmitt trigger output rails down to the Op-Amp power supply voltage $-V_{ss}$. The capacitor will start to charge down and its voltage V_C will swing down to reach $-V_{ss}$ with a characteristic time constant $\tau = RC$. Once $V_C \leq -V_{ss}/2$, the Schmitt trigger output will switch to $+V_{ss}$and the the capacitor voltage V_C will start swinging to $+V_{ss}$ with the same characteristic time constant τ. This cycle will keep repeating generating a square wave at the Schimtt trigger output.

The Period of the oscillation can be computed considering the time for exponential decay with time constant τ to go from $V_{ss}/2$ to $-V_{ss}/2$. After some algebra one obtains

$$T = 2\log(3)\,\tau$$

which shows in this case (same resistors on the positive feedback loop) that the period does not depend on the voltage limits but only on τ. In a more general case when the positive feedback loop resistors R_0 are different, T will depend also on the values of those resistors.

6.8 Problems Preparatory to the Laboratory

1. Replace a JFET amplifier of the phase shift oscillator with an Op-amp. Hint: the amplifier configuration must provide 180° of phase shift and the virtual ground can be used to simplify the feedback network and amplifier.
   Find the components values to satisfy the Barkhausen criterion for an oscillating frequency $\nu = 5$kHz.

2. Design a Wien bridge oscillator with a frequency of 1 kHz, 5kHz and 10kHz.

3. Using the expression of β, derive the resonance frequencies formulas of the Colpitts and the Harley for LC oscillators.

4. Determine the expression of the RC relaxation oscillator period T when the positive feedback loop resistors of figure 6.9 are different. Let's rename the feedback resistor R_f and the resistor from ground to the positive input R_+.

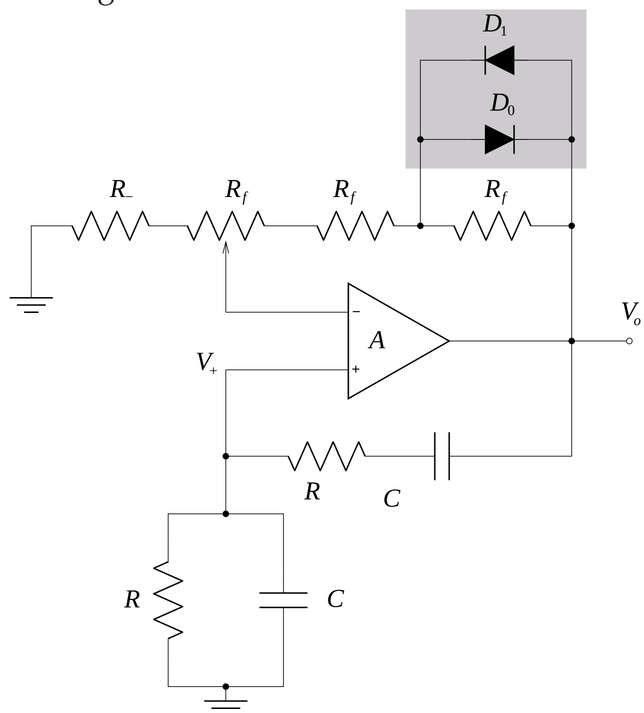
5. Design a RC relaxation oscillator with a frequency of 10 kHz, 100kHz and 500kHz.

6.9 Laboratory Procedure

Read carefully the entire procedure before starting the experiment.
Consult the data-sheet to properly connect the devices pin-out.
Before powering your circuit up, cross-check the power supply connections.
It is always a good practice to turn on the dual power supply at the same time to avoid potential damages of circuit components.
Note on your log book all the unpredicted behavior you experience in the circuits response.

1. Build a Wien bridge sinusoidal oscillator with a frequency ν between 1 kHz and 10 kHz with a μ741 Op-Amp. Use a potentiometer to match the resistances of the positive feedback network. Arrange more than one capacitor to obtain two capacitances with the same value. Neglect first the automatic gain control circuit highlighted in

the gray box in the figure below



(a) Measure the open loop transfer function $A(\omega)\beta(\omega)$ to verify the gain and phase around the resonance.

(b) Compare the measured oscillator frequency $\langle\omega_0\rangle_{Exp}$with the theoretical value ω_0.

(c) Check the behavior of the circuit when the open loop gain $A\beta$ is greater than one or smaller than one.

(d) Add the AGC circuit and tune the gain to properly sustain the oscillation.

(e) Verify that the oscillator can be tuned by changing the resistors or the capacitors pair.

(f) Measure the spectrum of your oscillator using the FFT math function of your oscilloscope or a laboratoty spectrum analyzer, and compute the total harmonic distortion

$$THD = \frac{1}{V_0^2}\sum_{n=1}^{N} V_n^2 ,$$

where V_n is the amplitude of the nth-harmonic frequency, V_0 is the amplitude of the fundamental frequency. N is determined by the required precision, and practically by the resolution of the instrument.

2. Build a RC relaxation oscillator with a frequency ν between 10 kHz and 500 kHz using an AD711. Verify that
   (a) the Schmitt trigger triggers properly,
   (b) the time constant $\langle\tau\rangle_{Exp}$ of the relaxation process equals RC,
   (c) oscillation frequency if matches the design.

Bibliography

[1] http://www.analog.com/UploadedFiles/Tutorials/450968421DDS_Tutorial_rev12-2-99.pdf

[2] Microelectronics, Jacob Millman, and Arvin Grabel , Mac-Graw Hill

Chapter 7

Phase Locked Loop (PLL)

A phase locked loop PLL[1] is a circuit with a feedback network that synchronizes an oscillator, the *reference oscillator* (REF), to another oscillator, the *controlled oscillator* (CO), so that they will oscillate (be locked together) at the same frequency.

The reader should familiarize with the acronyms as soon as possible.

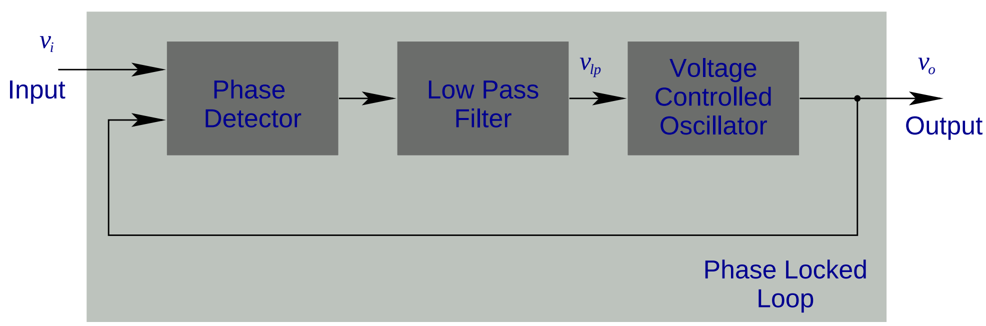


Figure 7.1: Phase-Locked loop block diagram.

To implement a PLL we need a circuit that generates a signal proportional to the phase difference between the REF and the CO. This continuously changing signal is then used to correct the frequency of the CO to be the same of the REF. In fact, if the phase difference is constant or zero the two oscillator must have the same frequency. In other words, keeping the phase differences constant makes the oscillator frequencies the same.

[1]It seems that the first phase locked loop was proposed by the French scientist De Belleseize in 1932.

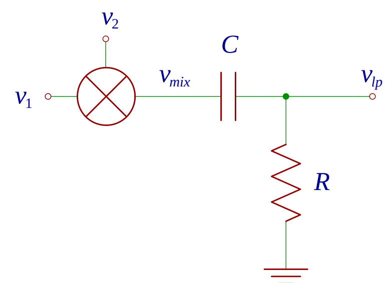


Figure 7.2: Mixer Phase-Detector and low-pass filter. The two cascaded circuits produce the error signal to be sent to the VCO.

Another way to see this is that the time variation of phase is proportional to the frequency difference between the oscillators, and therefore the phase difference is the signal we need to correct the change of frequency between the two oscillators.

LetŽs look the at Figure 7.1 containing the block diagram of a basic PLL. The reference signal from REF is sent to the PLL input, goes into the phase detector, which gives a signal proportional to the phase difference between the CO and the reference. This signal has high frequency noise and in general needs to be low pass filtered and compensated. Then, the filtered signal goes to the *voltage controlled oscillator* (VCO). The VCO, the core of the PLL, has a circuit to control the frequency by changing its voltage input. This input is therefore driven with a voltage with the proper sign to zero the phase difference between the reference frequency and the CO.

7.1 Phase Detector

Phase detectors convert the phase difference between two signal into a signal proportional to the phase difference.

Phase detectors can be classified into two types. Type I phase detectors are designed to be driven by analog signals, whereas Type II are driven by digital signal and in particular by the transitions/edges of such signals.

7.1.1 Type I Phase Detector, Analog Mixer

The analog mixer is a device that ideally multiplies two arbitrary signals. If the two signals are simple sinusoids with the same frequency, the output can be decomposed into two components as shown as follows. If the two input signals are

$$\begin{aligned} v_1 &= V_1 \sin(\omega t) , \\ v_2 &= V_2 \sin(\omega t + \delta\phi_0) , \end{aligned}$$

then after some algebra the multiplied signal v_{mix} (the mixer output) will be

$$v_{mix} = v_1\, v_2 = \frac{1}{2} V_1 V_2 \sin(\delta\phi_0) + \frac{1}{2} V_1 V_2 \sin(2\omega t + \delta\phi_0) .$$

The output of the mixer is therefore the phase difference of the two sinusoidal signals or their time integrated frequency difference plus a component at twice the frequency of $v_1$or v_2 . Applying an appropriate low pass filter we finally get our wished phase difference detector.

7.1.2 Type I Phase Detector, Logic Gates

Another basic type I phase detector is essentially a logic gate with a low-pass filter, the graph of the output voltage versus phase difference is as shown. The logic gate pulses which has a duration of the phase difference between the two input signals. Those pulses are the added together by the low pass filter producing a voltage which is proportional to the phase difference.

7.2 Voltage Controlled Oscillator (VCO)

As we already said before a voltage controlled oscillator is an oscillator whose frequency can be controlled by changing the voltage input.

A voltage controlled capacitance is useful for tuning applications.

7.3 Varactors or Varycap

A *varactor diode* or *varycap* is a voltage controlled capacitance. It is essentially a reverse biased p-n junction whose capacitance increase if the re-

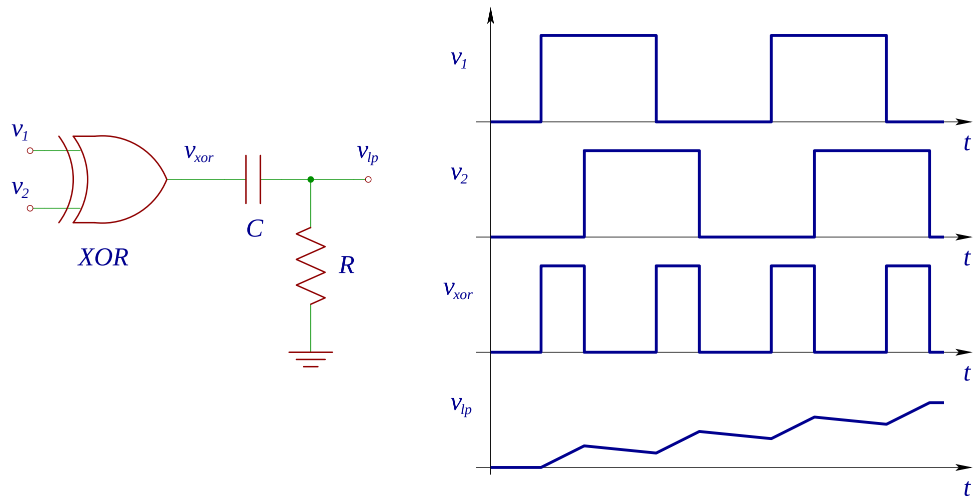


Figure 7.3: Phase-Detector and low-pass filter. The two cascaded circuits produce the error signal to be sent to the VCO.

verse bias decreases.

Intuitively, a reverse biased p-n junction is a capacitor with the depletion region acting as an insulator. Increasing the reverse bias the p-n depletion region increases and therefore the capacitance decrease. The major difference between a varactor and a diode is that the varactor is optimized to be a variable capacitance (as much as the technology allows) controlled with a bias.

Typical values are from tens to hundreds of picofarads. Because the small variation of capacitance available they cannot be effectively used at low frequency.

Varactors commonly available are the Motorola's MVAM115, and the Phillips BB112, BB212, BB204.

7.4 CMOS 4046 PLL Circuit

The CMOS 4046 PLL is a integrated circuit which implements a VCO an two PDs ans some extra circuits to simplify the construction of a PLL circuit.

The VCO frequency range is set with the components R_1, R_2, and C_1. Resistor R_1 and capacitor C_1 values set the maximum frequency f_{max} of

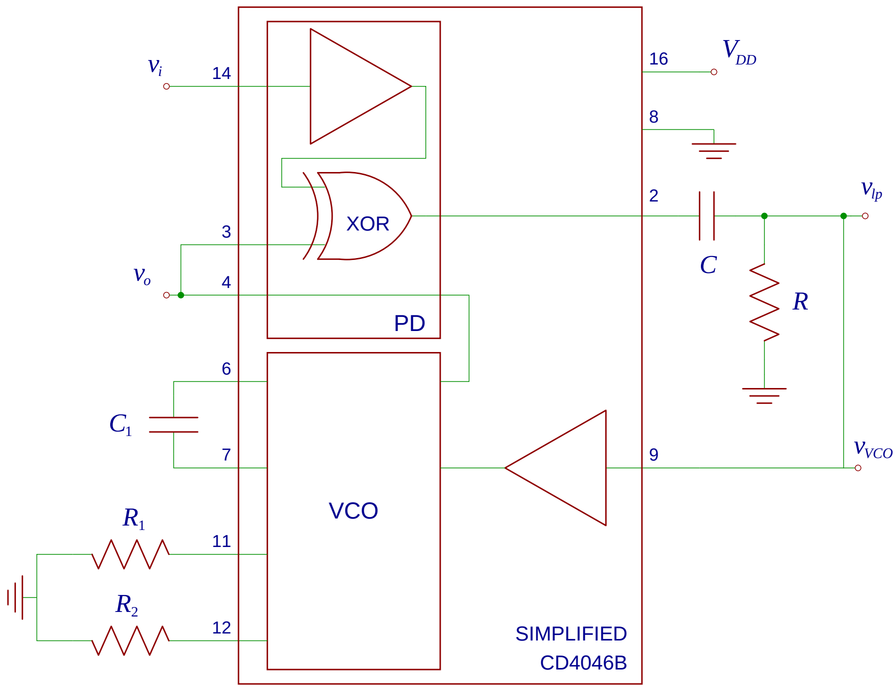


Figure 7.4: Simplified circuitry of the CMOS 4046 with components to set the VCO frequency range and the low-pass circuit compensating circuit.

the VCO. Resistor R_2 and Capacitor C_1 set an optional frequency offset f_{min}. The values limitations are:

- $5k\Omega \leq R_1 \leq 1M\Omega$
- $R_2 \leq 1M\Omega$
- $C_1 \geq 100pF, 5V \leq V_{DD} < 10V$
- $C_1 \geq 50pF, 10V \leq V_{DD} < 20V$

VCO input has a very high input impedance which allows to use a wide range of values for the capacitor C and the resistor R for the low-pass filter circuit.

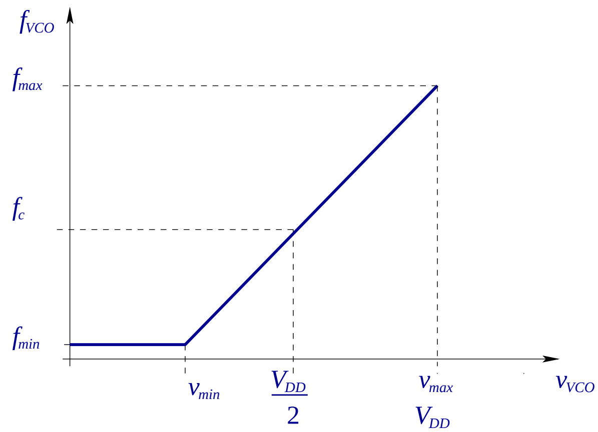


Figure 7.5: VCO characteristic of the CMOS 4046 .

7.5 Pre-lab Problems

- Determine the values of R_1, R_2, and C_1 to set the VCO frequency between 10 kHz and 15kHz. Use the CMOS 4046 data-sheet.
- Sketch the VCO characteristics for the previously selected VCO frequency range and for $V_{DD} = 12$V. Find the VCO gain K_0.
- Determine the value of the decoupling capacitor C_i for the previously selected VCO frequency range.
- Determine the value of the low-pass filter components R, C, for a cut-off frequency of 1 kHz.

7.6 Procedure

Circuit Setup

- Familiarize wit the PLL CMOS 4046 pin-out looking at its data-sheet. Mount the CMOS 4046 circuit with the value of R_1, R_2, and C_1 calculated in the pre-labs and $V_{DD} = 12$ V. Verify that the VCO minimum frequency f_{min} is approximately correct. Explain the behavior of VCO output when its input (PIN 9) is floating or grounded.

VCO Characteristics

- Measure f_{out} versus v_{in} VCO characteristics. Note that v_{in} can be varied between 0V to V_{DD}, and determine
  - v_{min}, f_{min}
  - v_{max}, f_{max}
  - f_c for $v_{in} = V_{DD}/2$
  - the VCO gain K_0, i.e. the slope of the linear range of the VCO characteristics

Phase Detector Characteristics

- Drive the PLL inputs (pin 14 and 3) manually with a varying voltage and and 4046a square wave. Verify that the output varies accordingly to the XOR response

VCO Closed Loop Characterization

- Verify the RC low-pass characteristics with the values of R, and C calculated in the pre-lab problems.
- Closed the PLL using the low-pass circuit you constructed and verify that the VCO output is phase locked to a function generator with a frequency set approximately to f_c.
- Vary the function generator frequency and verify that the loop is till working.
- Find the capture range varying the frequency of the function generator

Appendix A

Decibels

A.1 Definition of Bel and Decibel

The bel[1] is defined as the logarithm in base ten of a power P normalized to a reference power P_r , i.e.

$$X\,\mathrm{B} = \log_{10} \frac{P}{P_r}. \tag{A.1}$$

The decibel is 10 bels

$$X\,\mathrm{dB} = 10\,X\,\mathrm{B} = 10\,\log_{10} \frac{P}{P_r}. \tag{A.2}$$

Bels and decibels are dimensionless. The bel is not a unit, but a formula to conveniently scale homogeneous quantities thanks to the properties of the logarithmic function.

Bels are not commonly used because if we consider integer values of bels they do not provide a good resolution. We will just consider decibels for the remainder of this notes.

Considering that

$$P = \frac{V^2}{|Z|} = |Z|\,I^2,$$

and supposing that we use the same reference impedance magnitude $|Z_r|$

[1]The units scale "bell" was name after Alexandre Graham Bell, scientist and inventor.

for P, and P_r,we can rewrite equ. (A.2) as

$$X\,\text{dB} = 20\log_{10}\frac{V}{V_r} = 20\log_{10}\frac{I}{I_r},$$

where V_r, and I_r are respectively the voltage and the current across the reference impedance $|Z_r|$. In other words, we have to measure the voltage or the currents across equal impedances, to get the decibels.

A.2 Generalization of the Use of Decibel

For practical purposes, the decibel is also used to report the ratio of any homogeneous quantities such as the voltage output V_o over the voltage input V_i of a two port network, or in general, the ratio of any kind of homogeneous quantities x_1, x_2

$$X\,\text{dB} = 20\log_{10}\frac{x_1}{x_2}\,.$$

In this case there is no normalization respect to a reference load R_r or power P_r.

A.3 Useful Table and Properties

The next table is quite useful to easily translate decibels into magnitude

[dB]	**0**	1	2	3	4	5	**6**	7	8	9	**10**
Magnitude	**1**	1.1	1.2	1.4	1.6	1.8	**2**	2.2	2.5	2.8	**3.2**

For convenience, letŽs rewrite some useful properties of the logarithm function

$$\begin{aligned}
\log(x\,y) &= \log\,x + \log\,y,\\
\log(x/y) &= \log\,x - \log\,y,\\
\log x^n &= n\log\,x,\\
\log_a x &= \log_b x/\log_b a.
\end{aligned}$$

A.4 Standard Power References

Decibels comes in many flavors (different reference powers) depending on the application, radio frequency, microwaves, optics, acoustics, et cetera.

For example the following definition is quite often used

$$X\,\mathrm{dBm}(R_r) = 10\log_{10}\frac{V^2/R}{1\mathrm{mW}}$$

The value of R_r depends on the application field

	R_r [Ω]
Radio Frequency	50
TV Frequencies	75
Audio Frequencies	600

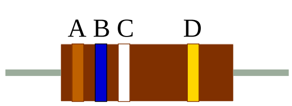
Appendix B

Resistor Color Code

Nominal values of resistances are coded using colors bands around the resistors (see figure below). The bands identify digits and the exponent in base ten for the resistance value and the tolerance as explained in the following table:

Band Number	1	2	3	4 (Tolerance band)	5
3 Bands	Digit	Digit	Exponent	Always 20%	
4 Bands	Digit	Digit	Exponent	Tolerance	
5 Bands	Digit	Digit	Exponent	Tolerance	Tolerance after 1000 hours

3 Band resistors have no band for the tolerance because it is assumed to be 20% of the nominal values.The fifth band is not an industry standard, but quite often it means the tolerance after 1000 hours of continuous use.



$$R = AB \cdot 10^C, \quad \Delta R = R \cdot D$$

The bands are counted from left to right. The following table reports the coding of the values using colors and a mnemonic sentence to remember the color code table.

Mnemonic Sentence	Color	Exponent	Tolerance (%)	Tolerance (%) 5th Band
Big	Black	0	20	
Bart	Brown	1	1	1%
Rides	Red	2	2	0.1%
Over	Orange	3		0.01%
Your	Yellow	4		0.001%
Grave	Green	5		
Blasting	Blue	6		
Violent	Violet	7		
Guns	Gray	8		
Wildly.	White	9		
Go	Gold	-1	5	
Shoot (him?)	Silver	-2	10	

For example, the nominal resistance of a 4 band resistor having the sequence brown, black, orange and gold is

$$\begin{aligned} R_{nom.} &= 10\,\mathrm{k}\Omega \\ \Delta R_{nom.} &= 5\%10\,\mathrm{k}\Omega \end{aligned} \quad \Rightarrow \quad R_{nom.} = (10.0 \pm 0.5)\ \mathrm{k}\Omega$$

Resistor size (volume) is related to the power dissipation capability. Typical used values are 1/8W, 1/4W, 1/2W, 1W.

Appendix C

The Cathode Ray Tube Oscilloscope

Every time we need to analyze or measure an electronic signal in the time domain we will probably use some type of oscilloscope. The oscilloscope is therefore one of the most useful tools used in a laboratory. Practically, it is an indispensable instrument for measuring, designing, manufacturing, or repairing electronic equipment.

Quite often, one can still find old Cathode Ray Tube (CRT) oscilloscopes even in modern laboratory, mainly because of the inadequacy of state of the art digital oscilloscope scopes to represent very fast signals. It is therefore worthwhile to study this device and understand how a CRT works and also its limitations.

C.1 The Cathode Ray Tube Oscilloscope

The *cathode ray tube oscilloscope* is essentially an analog[1] instrument that is able to measure time varying electric signals. It is made of the following functional parts (see figure C.1):

- the cathode ray tube (CRT),
- the trigger,

[1]Hybrid instruments combining the characteristics of digital and analog oscilloscopes, with a CRT, are also commercially available.

- the horizontal input,
- the vertical input,
- time base generator.

Let's study in more detail each component of the oscilloscope.

C.1.1 The Cathode Ray Tube

The CRT is a vacuum envelope hosting a device called *an electron gun* , capable of producing an electron beam, whose transverse position can be modulated by two electric signals (see figures C.1 and C.7).

When the electron gun cathode is heated by wire resistance because of the Joule effect it emits electrons . The increasing voltage differences between a set of shaped anodes and the cathode accelerates electrons to a terminal velocity v_0 creating the so called electron beam.

The beam then goes through two orthogonally mounted pairs of metallic plates. Applying voltage difference to those plates V_x and V_y, the beam is deflected along two orthogonal directions (x and y) perpendicular to its direction z. The deflected electrons will hit a plane screen perpendicular to the beam and coated with florescent layer. The electrons interaction with this layer generates photons, making the beam position visible on the screen.

C.1.2 The Horizontal and Vertical Inputs

The vertical and horizontal plates are independently driven by a variable gain amplifier to adapt the signals $v_x(t)$, and $v_y(t)$ to the screen range. A DC offset can be added to each input to position the signals on the screen. These two channels used to drive the signals to the plates signals are called horizontal and vertical inputs of the oscilloscope.

In this configuration the oscilloscope is an x-y plotter.

C.1.3 The Time base Generator

If we apply a sawtooth signal $V_x(t) = \alpha t$ to the horizontal input, the horizontal screen axis will be proportional to time t. In this case a signal $v_y(t)$

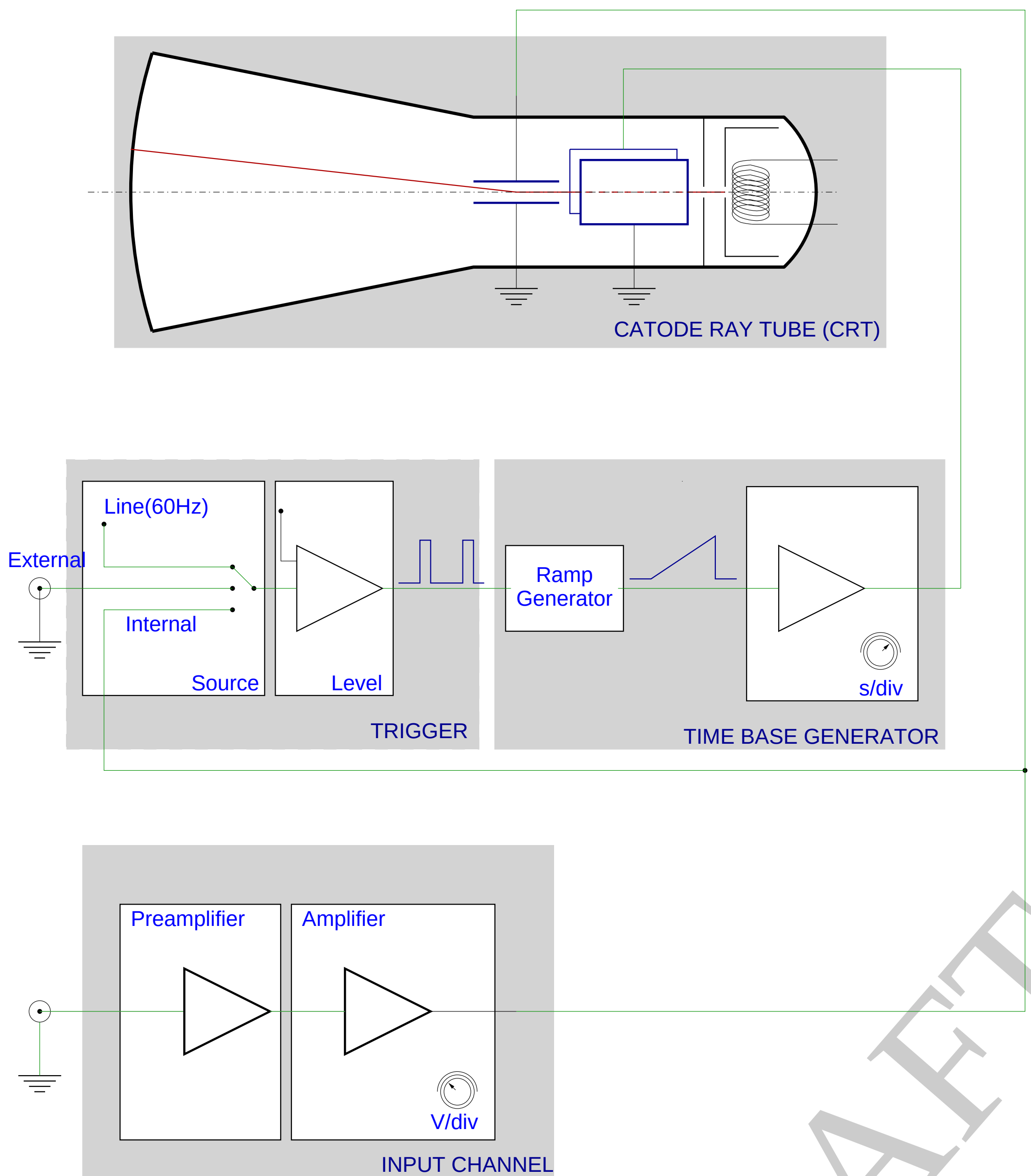


Figure C.1: Sketch of the functional parts of the analog oscilloscope, preamplifier, amplifier, trigger, time base generator, and CRT.

applied to the vertical input, will depict on the oscilloscope screen the signal time evolution.

The internal ramp signal is generated by the instrument with an amplification stage that allows changes in the gain factor α and the interval of time shown on the screen. This amplification stage and the ramp generator are called the *time base generator.*

In this configuration, the horizontal input is used as a second independent vertical input, allowing the plot of the time evolution of two signals.

Visualization of signal time evolution is the most common use of an oscilloscope.

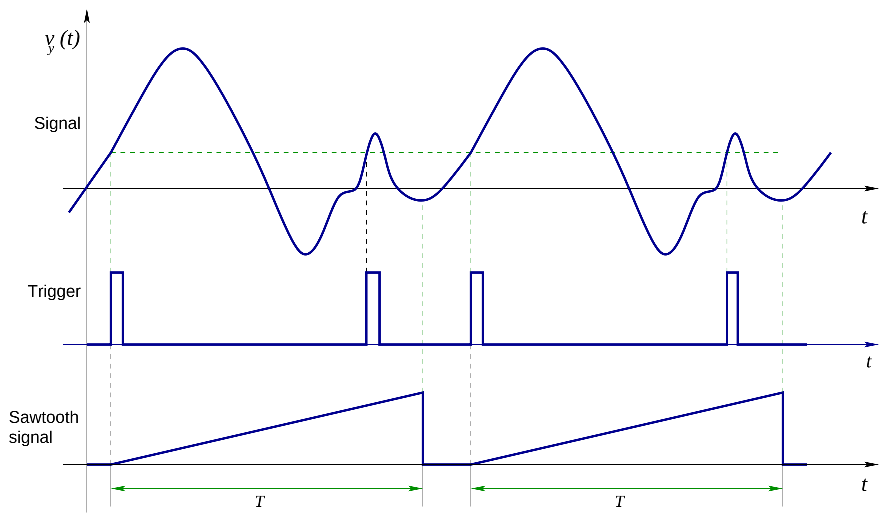


Figure C.2: Periodic Signal triggering.

C.1.4 The Trigger

To study a periodic signal $v(t)$ with the oscilloscope, it is necessary to synchronize the horizontal ramp $V_x = \alpha t$ with the signal to obtain a steady plot of the periodic signal. The trigger is the electronic circuit which provides this function. Let's qualitatively explain its behavior.

The trigger circuit compares $v(t)$ with a constant value and produces a pulse every time the two values are equal and the signal has a given slope. The first pulse triggers the start of the sawtooth signal of period[2] T

[2]In general, the sawtooth signal period T and the period of $v(t)$ are not equal.

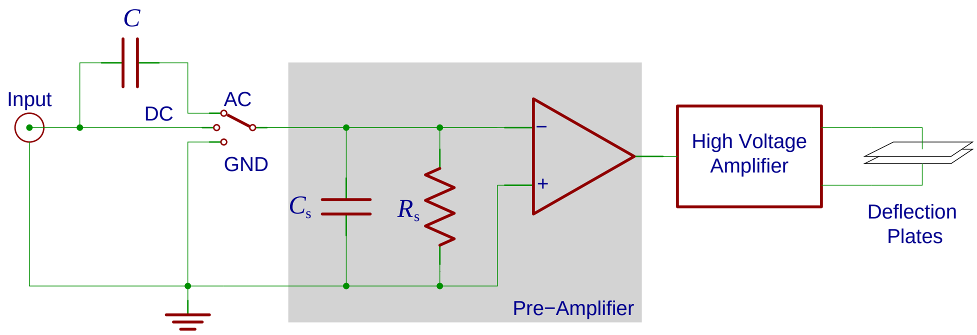


Figure C.3: Oscilloscope input impedance representation using ideal components (gray box). Input channel coupling is also shown.

, which will linearly increase until it reaches the value $V = \alpha T$, and then is reset to zero. During this time, the pulses are ignored and the signal $v(t)$ is plotted for a duration time T. After this time, the next pulse that triggers the sawtooth signal will happen for the same previous value and slope sign of $v(t)$, and the same portion of the signal will be re-plotted on the screen.

C.2 Oscilloscope Input Impedance

A good approximation of the input impedance of the oscilloscope is shown in the circuit of figure C.3. The different input coupling modes (DC AC GND) are also represented in the circuit.

The amplifying stage is modeled using an ideal amplifier (infinite input impedance) with a resistor and a capacitor in parallel to the amplifier input.

The switch allows to ground the amplifier input and indeed to vertically set the origin of the input signal (GND position), to directly couple the input signal (DC position), or to mainly remove the DC component of the input signal (AC position).

C.3 Oscilloscope Probe

An oscilloscope probe is a device specifically designed to minimize the capacitive load and maximize the resistive load added when the instrument is connected to the circuit. The price to pay is an attenuation of the signal that reaches the oscilloscope input[3].

Let's analyze the behavior of a passive probe. Figure C.4 shows the schematics of the equivalent circuit of a passive probe and of the input stage of an oscilloscope. The capacitance of the probe cable can be considered included in C_s

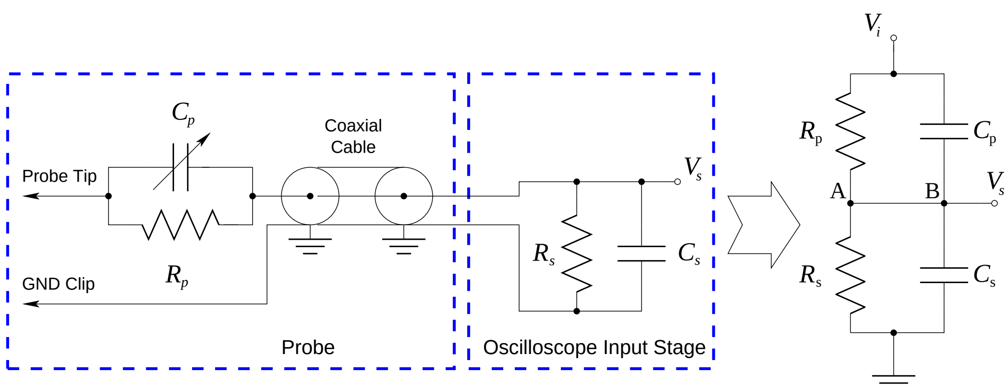


Figure C.4: Oscilloscope input stage and passive probe schematics.The equivalent circuit made of ideal components for the probe shielded cable is not shown.

Considering the voltage divider equation, we have

$$H(j\omega) = \frac{V_s}{V_i} = \frac{Z_s}{Z_p + Z_s}, \tag{C.1}$$

where

$$\frac{1}{Z_s} = j\omega C_s + \frac{1}{R_s}, \qquad \frac{1}{Z_p} = j\omega C_p + \frac{1}{R_p},$$

and then

$$Z_s = \frac{R_s}{j\omega\tau_s + 1}, \qquad Z_p = \frac{R_p}{j\omega\tau_p + 1}.$$

[3]Active probes can partially avoid this problems by amplifying the signal.

Defining the following parameters

$$\tau_p = C_p R_p, \quad \alpha = \frac{R_s}{R_s + R_p}, \qquad \beta = \frac{C_p}{C_s + C_p},$$

and after some tedious algebra, equation (C.1) becomes

$$H(j\omega) = \alpha \frac{1 + j\omega\tau_p}{1 + j\omega\frac{\alpha}{\beta}\tau_p},$$

which is the transfer function from the probe input to the oscilloscope input before the ideal amplification stage.

The DC and high frequency gain of the transfer function $H(j\omega)$ are respectively

$$H(0) = \alpha, \qquad H(\infty) = \beta.$$

The numerator and denominator of $H(j\omega)$ are respectively equal to zero, (the zeros and poles of H) when

$$\omega = \omega_z = j\frac{1}{\tau_p}, \qquad \omega = \omega_p = j\frac{\beta}{\alpha}\frac{1}{\tau_p}.$$

Figure C.5 shows the qualitative behavior of H for $\frac{\alpha}{\beta} > 1$.

C.3.1 Probe Frequency Compensation

By tuning the variable capacitor C_p of the probe, we can have three possible cases

$$\begin{aligned} \frac{\alpha}{\beta} < 1 \quad &\Rightarrow \quad \text{over-compensation} \\ \frac{\alpha}{\beta} = 1 \quad &\Rightarrow \quad \text{compensation} \\ \frac{\alpha}{\beta} > 1 \quad &\Rightarrow \quad \text{under-compensation} \end{aligned}$$

if $\alpha < \beta$ the transfer function attenuates more at frequencies above ω_z, and the input signal V_i is distorted.

if $\alpha = \beta$ the transfer function is constant and the input signal $V_i$will be undistorted, and attenuated by a factor α.

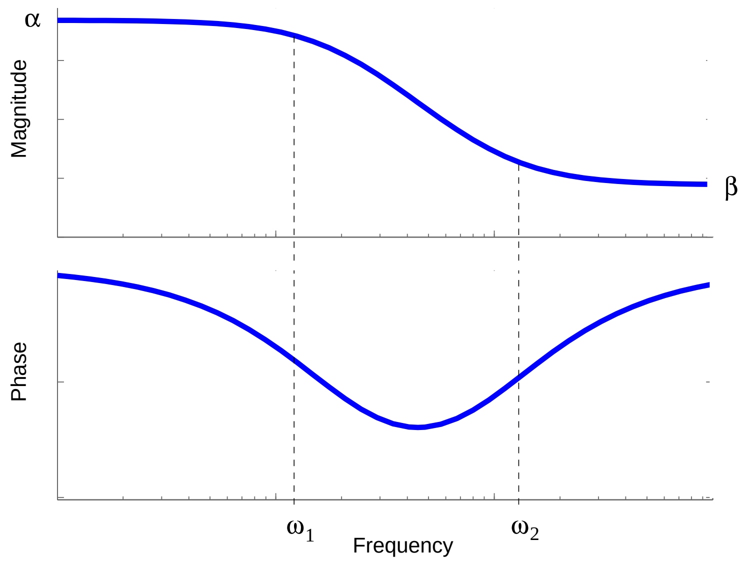


Figure C.5: Qualitative transfer function from the under compensated probe input to the oscilloscope input before the ideal amplification stage. As usual, the oscilloscope input is described having an impedance $R_s||C_s$.

if $\alpha > \beta$ the transfer function attenuates more at frequencies below ω_p and the input signal $V_i$is distorted.

The ideal case is indeed the compensated case, because we will have increased the input impedance by a factor α without distorting the signal.

The probe compensation can be tuned using a signal, which shows a clear distortion when it is filtered. A square wave signal is very useful in this case because, it shows a different distortion if the probe is under or over compensated. Figure C.6 sketches the expected square wave distortion for the two uncompensated cases.

It is worthwhile to notices that

$$\frac{\alpha}{\beta} = 1, \qquad \Rightarrow \frac{R_s}{R_p} = \frac{C_p}{C_s}.$$

This condition implies that:

- the voltage difference V_1 across R_s is equal the voltage difference V_2 across C_s, i.e $V_1 = V_2$

- the voltage difference V_3 across R_p is equal the voltage difference V_4 across C_p , i.e. $V_3 = V_4$
- and indeed $V_1 + V_2 = V_3 + V_4$.

This means that no current is flowing through the branch AB, and we can consider just the resistive branch of the circuit to calculate V_s. Applying the voltage divider equation, we finally get

$$V_s = \frac{R_s}{R_s + R} V_i$$

The capacitance of the oscilloscope does not affect the oscilloscope input anymore, and the oscilloscope+probe input impedance R_i becomes greater, i.e.

$$R_i = R_s + R_p.$$

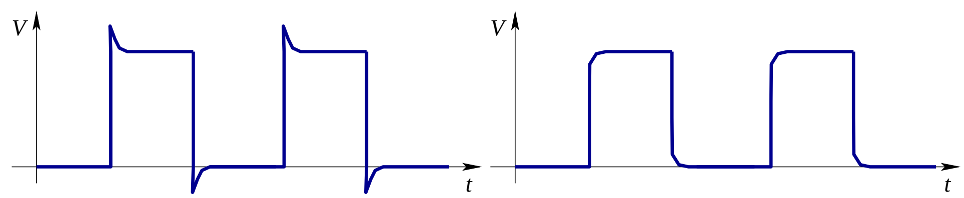


Figure C.6: Compensation of a passive probe using a square wave. Left figure shows an over compensated probe, where the low frequency content of the signal is attenuated. Right figure shows the under compensated case, where the high frequency content is attenuated.

C.4 Beam Trajectory

Let's consider the electron motion through one pair of plates.

The electron terminal velocity v_0 coming out from the gun can be easily calculated considering that its initial potential energy is entirely converted into kinetic energy, i.e

$$\frac{1}{2}\mu v_0^2 = eV_0, \quad \Rightarrow \quad v_0 = \sqrt{2\frac{eV_0}{\mu}},$$

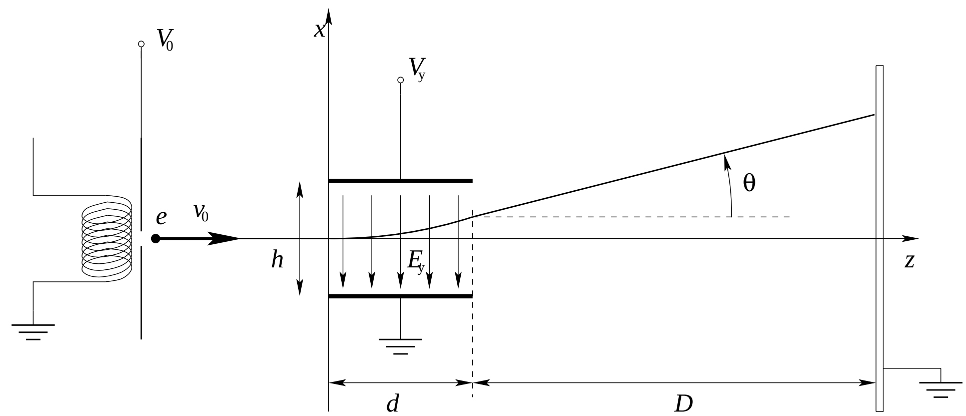


Figure C.7: CRT tube schematics. The electron enters into the electric field and makes a parabolic trajectory. After passing the electric field region it will have a vertical offset and deflection angle θ.

where μ is the electron mass, e the electron charge, and V_0 the voltage applied to the last anode.

If we apply a voltage V_y to the plates whose distance is h, the electrons will feel a force $F_y = eE_y$ due to an electric field

$$|E_y| = \frac{V_y}{h}.$$

The equation of dynamics of the electron inside the plates is

$$\begin{aligned} \mu\ddot{z} &= 0, \quad \Rightarrow \quad \dot{z} = v_0, \\ \mu\ddot{y} &= e|E_y|. \end{aligned}$$

Supposing that V_y is constant, the solution of the equation of motion will be

$$\begin{aligned} z(t) &= \sqrt{2\frac{eV_0}{\mu}}t, \\ y(t) &= \frac{1}{2}\frac{eV_y}{\mu h}t^2. \end{aligned}$$

Removing the dependency on the time t, we will obtain the electron beam trajectory , i.e.

$$y = \frac{1}{4h}\frac{V_y}{V_0}z^2,$$

which is a parabolic trajectory.

Considering that the electron is transversely accelerated until $z = d$, the total angular deflection θ will be

$$\tan\theta = \left(\frac{\partial y}{\partial z}\right)_{z=d} = \frac{1}{2}\frac{d}{h}\frac{V_y}{V_0}.$$

and displacement Y on the screen is

$$Y(V_y) = y(z = d) + \tan\theta D,$$

i.e.,

$$Y(V_y) = \frac{1}{2}\frac{d}{h}\frac{1}{V_0}(\frac{d}{2} + D)V_y.$$

Y is indeed proportional to the voltage applied to the plates through a rather complicated proportional factor.

The geometrical and electrical parameters of this proportional factor play a fundamental role in the resolution of the instrument. In fact, the smaller the distance h between the plates, or the smaller the gun voltage drop V_0, the larger is the displacement Y. Moreover, Y increases quadratically with the electron beam distance d.

C.4.1 CRT Frequency Limit

The electron transit time through the plates determine the maximum frequency that a CRT can plot. In fact, if the transit time τ is much smaller than the period T of the wave form $V(t)$, we have

$$V(t) \simeq \text{constant}, \qquad \text{if} \quad \tau \ll T,$$

and the signal is not distorted.

The transit time is

$$\tau = \frac{d}{v_0} = d\sqrt{\frac{\mu}{2eV_0}}.$$

Supposing that

$$\begin{cases} V_0 = 1\text{kV} \\ d = 20\text{mm} \\ \mu c^2 \simeq 0.5\text{MeV} \\ e = 1\text{eV} \end{cases} \quad \Rightarrow \quad \tau \simeq 1\text{ns}$$

Appendix D

Electromagnetic Field Noise

D.1 Introduction

Human and natural activities fill the surrounding space with electromagnetic fields (radiation) creating a very complex and unpredictable frequency spectrum of radiation. For example, domestic appliances, bulbs, fluorescent lights, and power line grids mainly irradiate at 60Hz and harmonics of 60Hz. Radios, televisions, wireless internet connections, and cellular phones networks are other typical sources, which fill the radiation spectrum from the kilohertz to the gigahertz region. Light mainly produced by the sun pervades the spectrum in the optical region. Radioactivity, gamma ray burst (GRB) emitted by astrophysical sources are for eaxmple responsible for filling the high and very high region of the spectrum.

Portion of this so complex spectrum can be attenuated by the so called electromagnetic shields but some others portions because of the energy involved cannot be effectively even attenuated.

The so called radio frequency noise can be easily attenuated (shielded) using a quite simple device known as the *Faraday cage*.

D.2 The Faraday Cage

Gauss's law states that a closed surface will prevent extern electrostatic fields from reaching the space enclosed by the surface. If the electric field is slowly varying i.e., its wavelength λ is large compared to the typical size d of the enclosure), then the field on the surface can be considered static and Gauss's law is then applicable. This enclosure is commonly called *Faraday cage*.

Using this crude approximation we can state that all frequencies much smaller than the following

$$\nu^* \sim \frac{c}{d}$$

where c is the speed of light, will be effectively attenuated. For example if $d = 1$ m then the Faraday cage will attenuate the external electromagnetic fields with frequencies much smaller than $\nu^* \sim 300$ MHz.

D.3 Practical Considerations

Normally, when we perform a measurement we cannot easily fit the lab in a small Faraday cage. Anyway, most of the time it is sufficient to enclose the physical system under measurement inside the cage . Then to perform the measurement we will have to connect the instrument sitting outside the cage to the system. The instruments leads acting like an antenna will still pick-up some of the ambient electromagnetic radiation. This effect can be amplified if we touch one of the leads increasing the antenna effect. A way to minimize this effect is to connect Faraday cages together. Reasonably good instruments have a built in Faraday cage connected to ground. Connecting the cages to ground will create a more or less single effective cage which will attenuate the electromagnetic noise pick-up.

Appendix E

Common Emitter BJT Amplifier

The common emitter BJT amplifier is one of the most simple design that allows to set the voltage amplification A_v quite independently from the BJT characteristics.

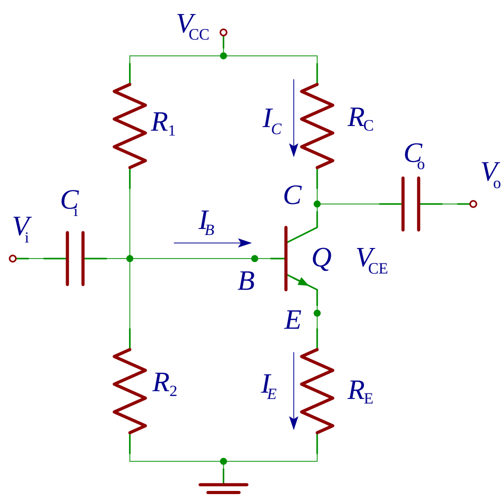


Figure E.1: BJT Common emitter amplifier with coupling capacitors C_i, and C_o.

To properly set the BJT working point, we have to forward bias the emitter base junction and reverse bias the collector base junction. But this is not enough if we want to build an amplifier. The other requirement is to set the voltage V_{CE} where the VCE characteristic is flat and wide enough

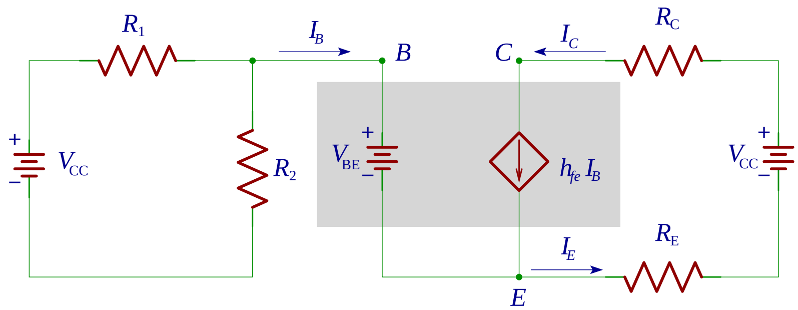


Figure E.2: Common emitter equivalent circuit which simplifies the BJT biasing understanding.

to accommodate the output signal excursion. In other words, we donŽt want the output to swing into the BJT saturation region or into the break down region.

The design parameters we have to set are are A_v, I_C,V_{CE},V_{CC}, and essentially, the VCE characteristics contains all the information we need to properly bias the BJT. As last remark, voltage gain and bias point are "intimately" related and cannot be completely independent.

E.1 Amplifier Design

The analysis of the circuit becomes quite easy if we observe from the V_{CE} characteristic that

$$I_C \gg I_B\,. \tag{E.1}$$

Applying KVL to the output mesh, we will have

$$V_{CC} = R_C I_C + R_E I_E + V_{CC} \simeq (R_C + R_E)\, I_C + V_{CE} \tag{E.2}$$

If we want to optimize the dynamic range of the amplifier, and neglecting the saturation region, we will have to set according to the $I_C - V_{CE}$ characteristic

$$V_{CE} \simeq \frac{1}{2} V_{CC}$$

Using this design condition and and voltage gain of this circuit we will have

$$R_E = \frac{1}{2\,(1+A_v)} \frac{V_{CC}}{I_C}$$

This equations together with the gain equation (E.8) set the values R_C and R_E based only on the design parameters V_{CC},I_C, and A_v. Let's now find the values of the voltage divider which forward bias the base-emitter junction.

If I_B is negligible, then resistors R_1 and R_2 act as a simple voltage divider, i.e.

$$V_B \simeq \frac{R_2}{R_1 + R_2} V_{CC}\,. \tag{E.3}$$

and for KVL

$$V_B = V_{BE} + R_E I_E \simeq V_{BE} + R_E I_C$$

where V_{BE} must be the voltage drop of a forward polarized diode junction, typically between 6.0 V to 0.7 V.

Using the two expressions of V_B and after some algebra, we get

$$R_1 \simeq R_2 \left(\frac{V_{CC}}{V_{BE} + R_E I_C} - 1 \right)\,.$$

E.2 Resume

Summarizing the results we have for $I_C \gg I_B$

$$\alpha = \frac{1}{2\,(1 + A_v)} \tag{E.4}$$

$$R_E = \alpha \frac{V_{CC}}{I_C} \tag{E.5}$$

$$R_C = A_v R_E \tag{E.6}$$

$$R_1 = \left(\frac{V_{CC}}{V_{BE} + \alpha V_{CC}} - 1 \right) R_2 \tag{E.7}$$

E.3 Example

LetŽs set the following design values

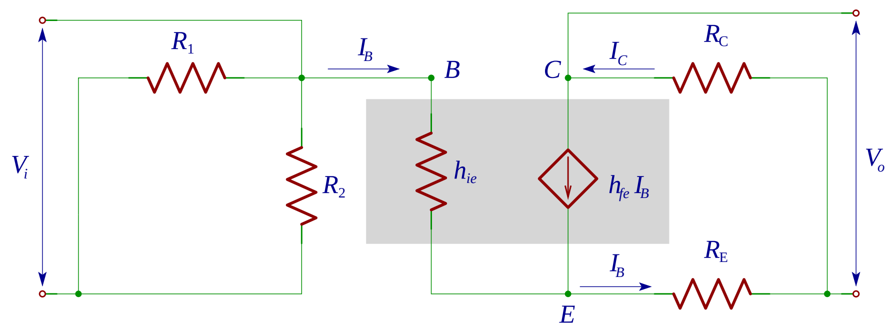


Figure E.3: Small signal circuit model for the common emitter BJT amplifier

$$\begin{cases} A_v & = & 10 \\ V_{CC} & = & 20\ \text{V} \\ I_C & = & 1\ \text{mA} \\ R_2 & = & 40\,\text{k}\Omega \end{cases} \quad \Rightarrow \quad \begin{cases} R_1 & \simeq & 452\,\text{k}\Omega \\ R_2 & \simeq & 40\,\text{k}\Omega \\ R_C & \simeq & 909\,\Omega \\ R_E & \simeq & 91\,\Omega \end{cases}$$

E.4 Amplifier Gain and Sign

Using the equivalent small signal circuit model for the BJT and considering the impedance of the ideal voltage and current sources we can construct the circuit show in figure E.3. Then from that figure it is finally easy to compute the voltage gain A_v and the input and output impedance R_i and R_o of the circuit.

In fact, considering that $I_B \ll I_C, R_E \gg h_{ie}$, the input and the output voltage are simply

$$\begin{cases} V_i & = & (h_{ie} + R_E)\, I_E \simeq R_E I_C \\ \\ V_o & = & R_C I_C \end{cases} , \Rightarrow A_v \simeq \frac{R_C}{R_E} \tag{E.8}$$

The Common Emitter BJT amplifier is an inverting stage. In fact, considering that

$$V_o = V_{CC} - (R_E + R_C)\, I_C \qquad \Rightarrow \qquad V_{CC} = V_o + (R_E + R_C)\, I_C$$

if I_C increases, then V_o must decrease to keep V_{CC} constant. If, we start with an input current and voltage in phase they will end up beeing out of phase by 180° degrees.

E.5 Input and Output Impedance

The input impedance is the impedance seen from the inputs lead , and can be easily computed considering that the ideal current source is an open circuit, i.e.

$$R_i = R_2 || R_1 || (h_{ie} + R_e)$$

The output impedance is then

$$R_o = R_C$$

E.6 I/O Coupling Capacitors

The coupling capacitors C_i will provide a way to send the input signal to amplifier without perturbing the DC bias of the BJT. Similarly, placing the capacitor C_o to the output will allow to connect a load without perturbing the DC bias of the BJT circuit.

Coupling capacitance should be selected to minimize the filtering effect on the amplifier response. For example, C_i will create a RC high pass filter with the R being the input resistance of the amplifier and C_o will do the same with the eventual resistance of the amplifier load.

E.7 Emitter Bypass Capacitor

Adding a so called bypass capacitor C_E in parallel with R_E will not change the DC bias of the BJT and will provide a the maximum possible voltage gain at high frequency as seen in the simple BJT amplifier circuit

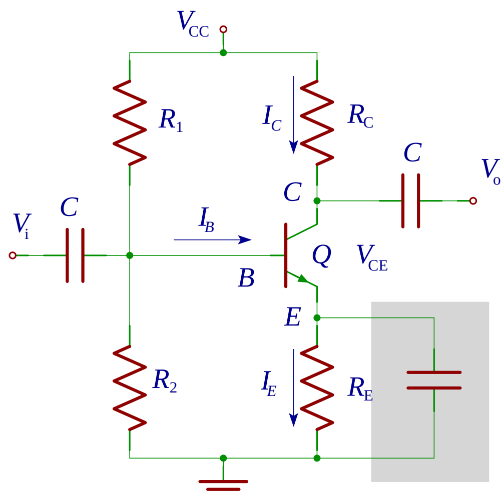


Figure E.4: BJT Common emitter amplifier with emitter bypassing capacitor.