



Sophomore Physics Laboratory (PH005/105)

Analog Electronics Phase Locked Loop (PLL)

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Chapter 8

Phase Locked Loop (PLL)

A phase locked loop PLL¹ is a circuit with a feedback network that synchronizes an oscillator, the *reference oscillator* (REF), to another oscillator, the *controlled oscillator* (CO), so that they will oscillate (be locked together) at the same frequency.

The reader should familiarize with the acronyms as soon as possible.

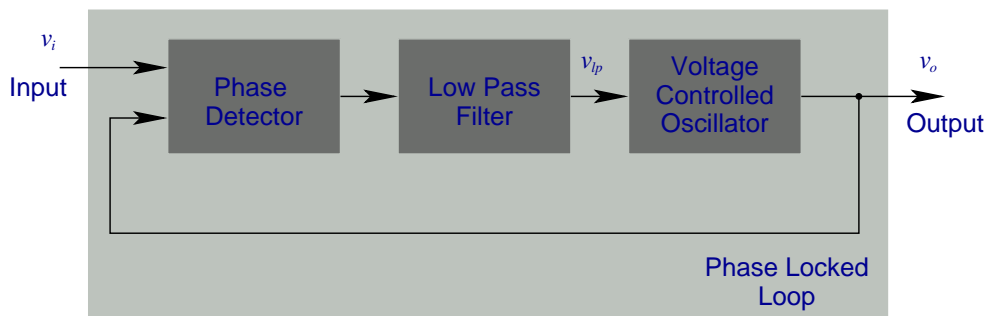


Figure 8.1: Phase-Locked loop block diagram.

To implement a PLL we need a circuit that generates a signal proportional to the phase difference between the REF and the CO. This continuously changing signal is then used to correct the frequency of the CO to be the same of the REF. In fact, if the phase difference is constant or zero the two oscillator must have the same frequency. In other words, keeping the phase differences constant makes the oscillator frequencies the same.

¹It seems that the first phase locked loop was proposed by the French scientist De Bellesize in 1932.

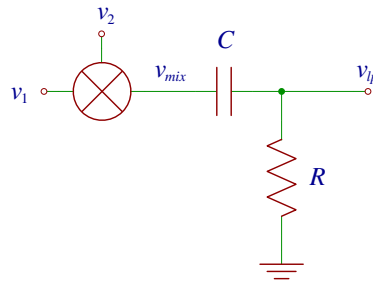


Figure 8.2: Mixer Phase-Detector and low-pass filter. The two cascaded circuits produce the error signal to be sent to the VCO.

Another way to see this is that the time variation of phase is proportional to the frequency difference between the oscillators, and therefore the phase difference is the signal we need to correct the change of frequency between the two oscillators.

Let's look at Figure 8.1 containing the block diagram of a basic PLL. The reference signal from REF is sent to the PLL input, goes into the phase detector, which gives a signal proportional to the phase difference between the CO and the reference. This signal has high frequency noise and in general needs to be low pass filtered and compensated. Then, the filtered signal goes to the *voltage controlled oscillator* (VCO). The VCO, the core of the PLL, has a circuit to control the frequency by changing its voltage input. This input is therefore driven with a voltage with the proper sign to zero the phase difference between the reference frequency and the CO.

8.1 Phase Detector

Phase detectors convert the phase difference between two signal into a signal proportional to the phase difference.

Phase detectors can be classified into two types. Type I phase detectors are designed to be driven by analog signals, whereas Type II are driven by digital signal and in particular by the transitions/edges of such signals.

8.1.1 Type I Phase Detector, Analog Mixer

The analog mixer is a device that ideally multiplies two arbitrary signals. If the two signals are simple sinusoids with the same frequency, the output can be decomposed into two components as shown as follows. If the two input signals are

$$\begin{aligned}v_1 &= V_1 \sin(\omega t), \\v_2 &= V_2 \sin(\omega t + \delta\phi_0),\end{aligned}$$

then after some algebra the multiplied signal v_{mix} (the mixer output) will be

$$v_{mix} = v_1 v_2 = \frac{1}{2} V_1 V_2 \sin(\delta\phi_0) + \frac{1}{2} V_1 V_2 \sin(2\omega t + \delta\phi_0).$$

The output of the mixer is therefore the phase difference of the two sinusoidal signals or their time integrated frequency difference plus a component at twice the frequency of v_1 or v_2 . Applying an appropriate low pass filter we finally get our wished phase difference detector.

8.1.2 Type I Phase Detector, Logic Gates

Another basic type I phase detector is essentially a logic gate with a low-pass filter, the graph of the output voltage versus phase difference is as shown. The logic gate pulses which has a duration of the phase difference between the two input signals. Those pulses are the added together by the low pass filter producing a voltage which is proportional to the phase difference.

8.2 Voltage Controlled Oscillator (VCO)

As we already said before a voltage controlled oscillator is an oscillator whose frequency can be controlled by changing the voltage input.

A voltage controlled capacitance is useful for tuning applications.

8.3 Varactors or Varycap

A *varactor diode* or *varycap* is a voltage controlled capacitance. It is essentially a reverse biased p-n junction whose capacitance increase if the re-

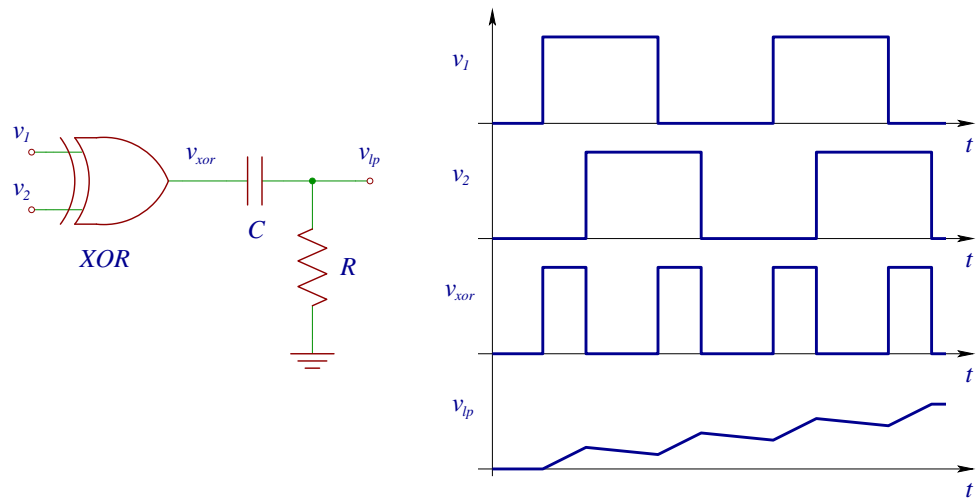


Figure 8.3: Phase-Detector and low-pass filter. The two cascaded circuits produce the error signal to be sent to the VCO.

verse bias decreases.

Intuitively, a reverse biased p-n junction is a capacitor with the depletion region acting as an insulator. Increasing the reverse bias the p-n depletion region increases and therefore the capacitance decrease. The major difference between a varactor and a diode is that the varactor is optimized to be a variable capacitance (as much as the technology allows) controlled with a bias.

Typical values are from tens to hundreds of picofarads. Because the small variation of capacitance available they cannot be effectively used at low frequency.

Varactors commonly available are the Motorola's MVAM115, and the Phillips BB112, BB212, BB204.

8.4 CMOS 4046 PLL Circuit

The CMOS 4046 PLL is a integrated circuit which implements a VCO an two PDs ans some extra circuits to simplify the construction of a PLL circuit.

The VCO frequency range is set with the components R_1 , R_2 , and C_1 . Resistor R_1 and capacitor C_1 values set the maximum frequency f_{max} of

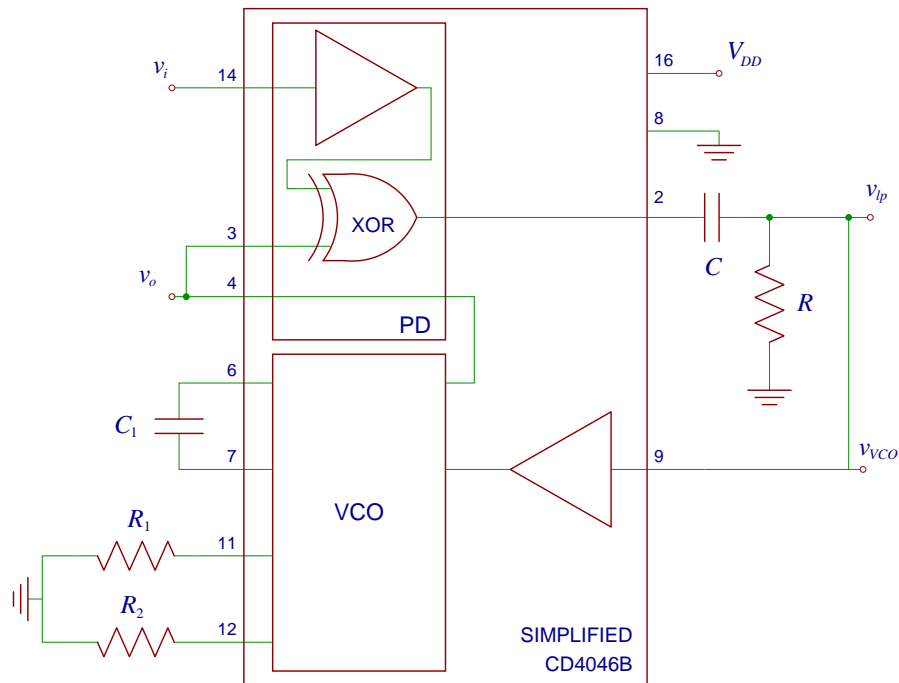


Figure 8.4: Simplified circuitry of the CMOS 4046 with components to set the VCO frequency range and the low-pass circuit compensating circuit.

the VCO. Resistor R_2 and Capacitor C_1 set an optional frequency offset f_{min} . The values limitations are:

- $5\text{k}\Omega \leq R_1 \leq 1\text{M}\Omega$
- $R_2 \leq 1\text{M}\Omega$
- $C_1 \geq 100\text{pF}, 5\text{V} \leq V_{DD} < 10\text{V}$
- $C_1 \geq 50\text{pF}, 10\text{V} \leq V_{DD} < 20\text{V}$

VCO input has a very high input impedance which allows to use a wide range of values for the capacitor C and the resistor R for the low-pass filter circuit.

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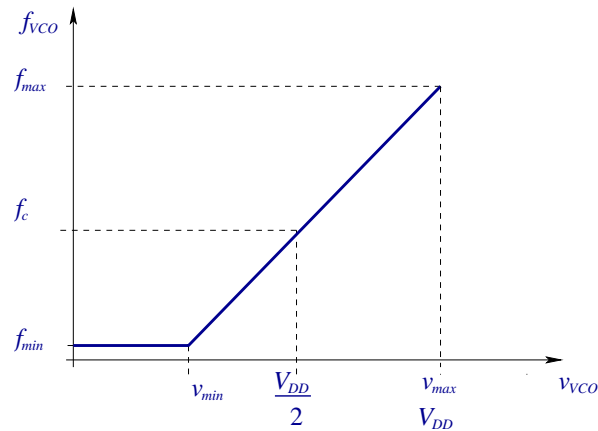


Figure 8.5: VCO characteristic of the CMOS 4046 .

8.5 Pre-lab Problems

- Determine the values of R_1 , R_2 , and C_1 to set the VCO frequency between 10 kHz and 15kHz. Use the CMOS 4046 data-sheet.
- Sketch the VCO characteristics for the previously selected VCO frequency range and for $V_{DD} = 12V$. Find the VCO gain K_0 .
- Determine the value of the decoupling capacitor C_i for the previously selected VCO frequency range.
- Determine the value of the low-pass filter components R , C , for a cut-off frequency of 1 kHz.

8.6 Procedure

Circuit Setup

- Familiarize with the PLL CMOS 4046 pin-out looking at its data-sheet. Mount the CMOS 4046 circuit with the value of R_1 , R_2 , and C_1 calculated in the pre-labs and $V_{DD} = 12 V$. Verify that the VCO minimum frequency f_{min} is approximately correct. Explain the behavior of VCO output when its input (PIN 9) is floating or grounded.

VCO Characteristics

- Measure f_{out} versus v_{in} VCO characteristics. Note that v_{in} can be varied between 0V to V_{DD} , and determine
 - v_{min}, f_{min}
 - v_{max}, f_{max}
 - f_c for $v_{in} = V_{DD}/2$
 - the VCO gain K_0 , i.e. the slope of the linear range of the VCO characteristics

Phase Detector Characteristics

- Drive the PLL inputs (pin 14 and 3) manually with a varying voltage and a 4046a square wave. Verify that the output varies accordingly to the XOR response

VCO Closed Loop Characterization

- Verify the RC low-pass characteristics with the values of R , and C calculated in the pre-lab problems.
- Close the PLL using the low-pass circuit you constructed and verify that the VCO output is phase locked to a function generator with a frequency set approximately to f_c .
- Vary the function generator frequency and verify that the loop is still working.
- Find the capture range by varying the frequency of the function generator

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