

# LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

**-LIGO-**

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	<b>DRAFT</b>	
<b>Lasti Ponderomotive Experiment Digital Controls Design</b>		
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# 1 Scope

The scope of this document is the digital controls design for the CDS control and monitoring of the Lasti Ponderomotive Experiment. Covered in this scope are all of the analog to digital converters required and their connection interfaces, computers and software, and digital connections to the Lasti CDS infrastructure. Specifically excluded are any analog signal conditioning units required and field cabling to the sensors and actuators (covered under separate documentation).

# 2 Purpose

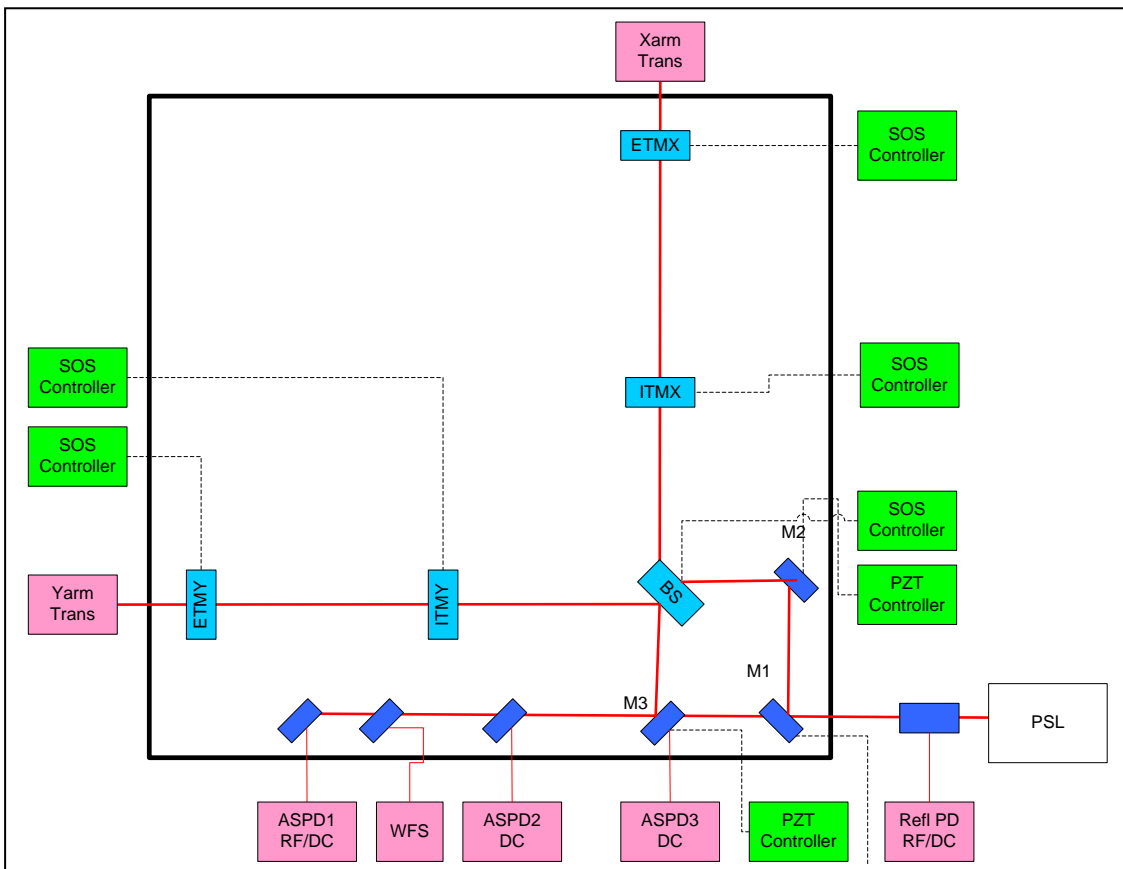
The purpose of this document is to describe a CDS design for the digital hardware and software required to control and monitor the Lasti Ponderomotive experiment.

# 3 References

1) LIGO T060031-00-C LASTI Digital Control and Data System (CDS) Design

# 4 Overview

Over the course of the next year, a Ponderomotive experiment will be conducted at the Lasti facility. An overview of the experiment components and layout are shown in the following figure..



To support this effort, CDS equipment will be provided, with installation to begin in the summer of 2006. As indicated by the diagram, the CDS must provide for control, monitoring and integration of several components:

- Suspended Optics Controls: Five small optic suspension (SOS) controllers will be provided, similar to the present Ligo SOS controllers.
- Alignment Sensing and Control: One WaveFront Sensors (WFS) is to be used to present alignment information.
- Length Sensing and Control (LSC): A total of six photodiodes, two RF/DC and four DC, will provide for length sensing and normalization.

As part of the requirements, all of the control loops involved in this system must run at 64KHz. In the future, it is likely that this rate will need to increase to 128KHz to control optical spring effects at 5KHz.

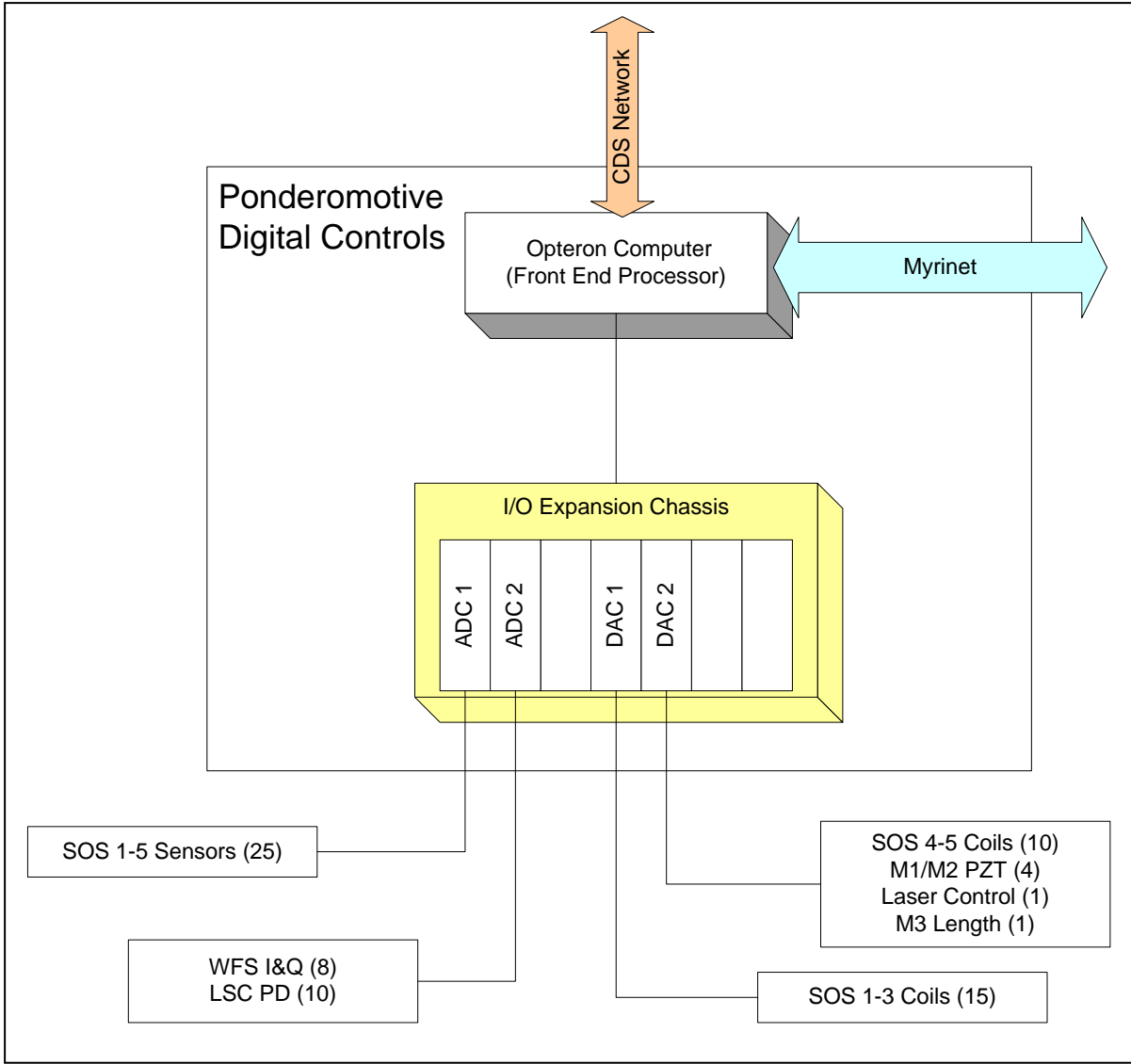
## 5 CDS Hardware

The CDS hardware implementation will follow the PCI design concepts for Lasti described in Reference 1. The specific digital hardware components for this CDS subsystem include:

- One multi AMD64 (Opteron) computer
- One PCI-X expander chassis
- Two ADC modules
- Two DAC modules
- One MyriNet Network Interface Card (NIC)

A sketch of the Ponderomotive control components and their interconnection are shown in the following figure.

Four of the seven available slots of the PCI-X expansion chassis are accounted for here. However, this is not yet a final count. There will be some additional TBD channels required, such as for switching of suspension whitening filters, that will require a digital I/O module and perhaps some additional ADC/DAC channels.



## 5.1 Analog Signal Connections

Analog signals will be connected to the digital I/O modules via cabling from the analog signal conditioning units. The signal connections to the ADC and DAC modules are given in the following tables. Along with the signals listed, timing clocks from the Lasti timing system will also be provided to all ADC/DAC modules via the analog conditioning units. Multiple digital I/O modules will also be provided to switch analog whitening and dewatering filters (not shown). *Note that this signal list is preliminary and provided at this time primarily for channel counting purposes.*

ADC MODULE 1 – SOS Sensor Signals			
Ch.	Signal	Ch.	Signal
00	ETMX UL Sensor	16	ETMY UL Sensor
01	ETMX UR Sensor	17	ETMY UR Sensor
02	ETMX LL Sensor	18	ETMY LL Sensor
03	ETMX LR Sensor	19	ETMY LR Sensor

04	ETMX Side Sensor	20	ETMY Side Sensor
05	ITMX UL Sensor	21	ITMY UL Sensor
06	ITMX UR Sensor	22	ITMY UR Sensor
07	ITMX LL Sensor	23	ITMY LL Sensor
08	ITMX LR Sensor	24	ITMY LR Sensor
09	ITMX Side Sensor	25	ITMY Side Sensor
10	BS UL Sensor	26	NC
11	BS UR Sensor	27	NC
12	BS LL Sensor	28	NC
13	BS LR Sensor	29	NC
14	BS Side Sensor	30	NC
15	NC	31	One PPS Timing Signal

<b>ADC MODULE 2 – WFS and LSC Sensor Signals</b>			
<b>Ch.</b>	<b>Signal</b>	<b>Ch.</b>	<b>Signal</b>
00	WFS5 I1	16	ASPD1 I
01	WFS5 I2	17	ASPD1 Q
02	WFS5 I3	18	ASPD1 DC
03	WFS5 I4	19	NC
04	WFS5 Q1	20	REFL PD I
05	WFS5 Q2	21	REFL PD Q
06	WFS5 Q3	22	REFL PD DC
07	WFS5 Q4	23	NC
08	NC	24	ASPD2 DC
09	NC	25	ASPD3 DC
10	NC	26	Xarm Trans
11	NC	27	Yarm Trans
12	NC	28	NC
13	NC	29	NC
14	NC	30	NC
15	NC	31	NC

<b>DAC MODULE 1 – ETMX, ETMY, BS Coil Drives</b>			
<b>Ch.</b>	<b>Signal</b>	<b>Ch.</b>	<b>Signal</b>
00	ETMX UL Coil	08	ETMY LR Coil
01	ETMX UR Coil	09	ETMY Side Coil
02	ETMX LL Coil	10	NC
03	ETMX LR Coil	11	BS UL Coil
04	ETMX Side Coil	12	BS UR Coil
05	ETMY UL Coil	13	BS LL Coil
06	ETMY UR Coil	14	BS LR Coil
07	ETMY LL Coil	15	BS Side Coil

<b>DAC MODULE 2</b>			
<b>Ch.</b>	<b>Signal</b>	<b>Ch.</b>	<b>Signal</b>
00	ITMX UL Coil	08	ITMY LR Coil
01	ITMX UR Coil	09	ITMY Side Coil
02	ITMX LL Coil	10	M1 PZT Pitch
03	ITMX LR Coil	11	M1 PZT Yaw
04	ITMX Side Coil	12	M2 PZT Pitch

05	ITMY UL Coil	13	M2 PZT Yaw
06	ITMY UR Coil	14	Laser Control
07	ITMY LL Coil	15	M3 LSC

## 5.2 Digital Signal Connections

Two digital signal paths exist to/from the front end control computer. All realtime network traffic, including data acquisition, is routed through the CDS Myrinet fabric. The front end computer will be connected to this network via a pair of multi-mode fiber optic cables.

Data acquisition and storage will be provided by the Lasti FrameBuilder. For purposes of connection within the Lasti DAQ system, this front end computer will be designated with a Data Collection Unit Identification (DCUID) number of 11.

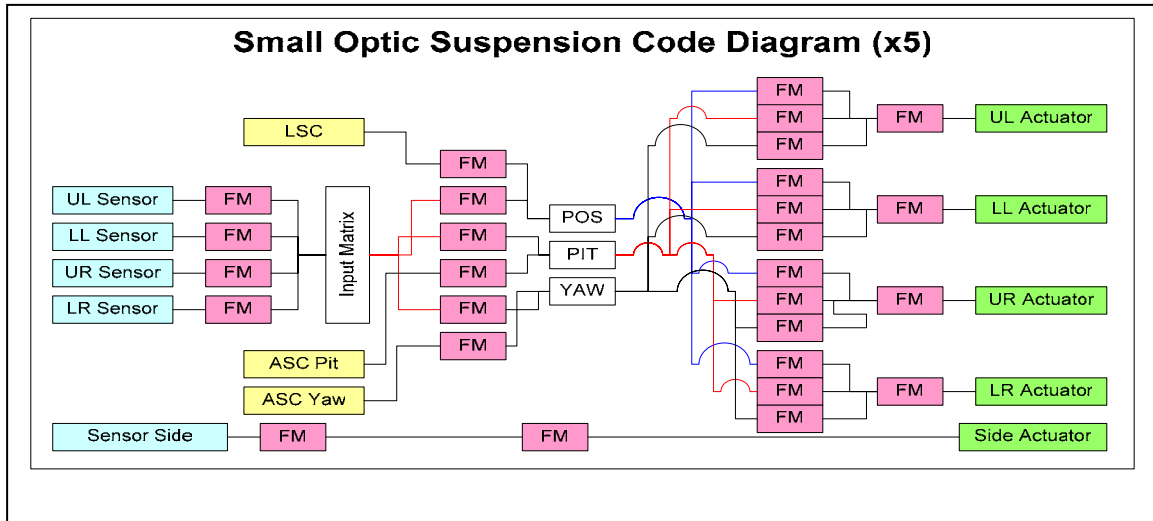
For transmission of EPICS data and other non-realtime communications, the front computer will be connected to the Lasti CDS Ethernet. This is a 100baseT copper wire connection via an RJ45 connector.

## 6 Software

The Ponderomotive front end control software will make use of the basic control code libraries developed for PCI based systems, as further described in Reference 1. It will also make use of CDS standard components previously developed for Ligo controls, such as the CDS standard IIR filter module.

### 6.1 Small Optics Control Software

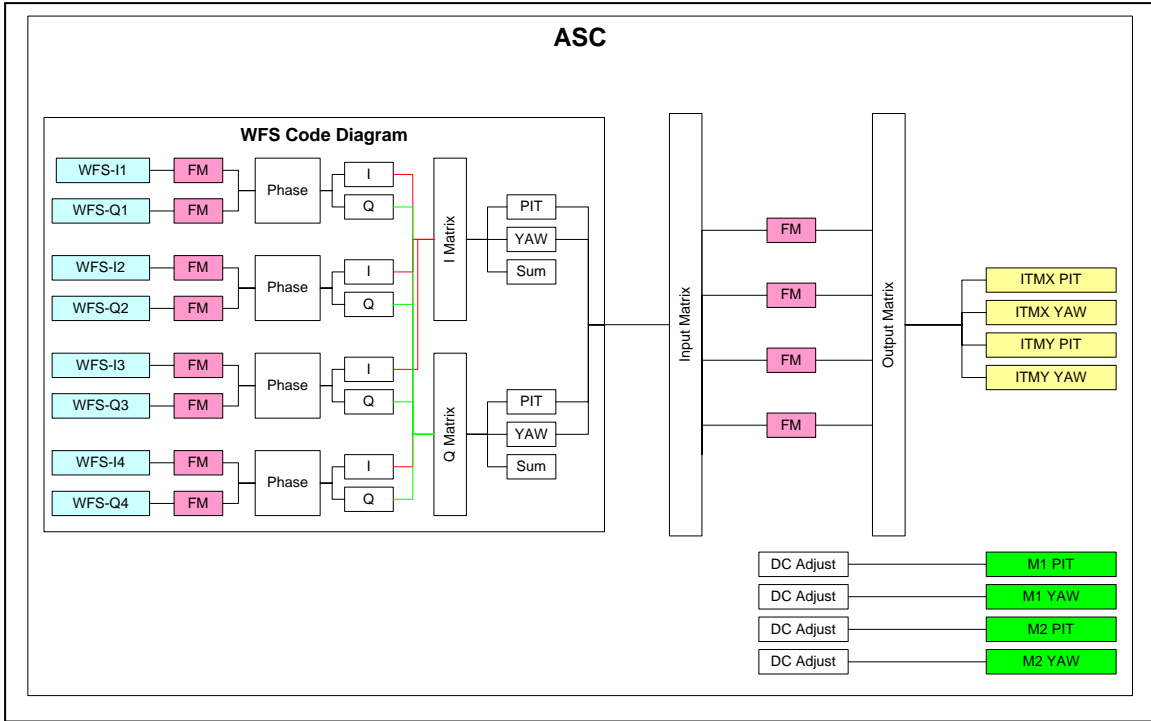
It is intended that the SOS control software be identical to that used in Ligo. A block diagram of that software is shown in the figure below. This code block is replicated five times for the five SOS controllers. Note that in this diagram, and others that follow, that ADC inputs are shown in blue, DAC outputs in green and internal software connections in yellow.



### 6.2 ASC Software

The software for the ASC portion of control is again similar to that of Ligo ASC systems. A basic block diagram is shown in the following figure. It consists of a single WFS input section code block, followed by a matrix and four DOF filter modules. The outputs of the system feed the pitch and yaw inputs of the two ITM suspension controls.

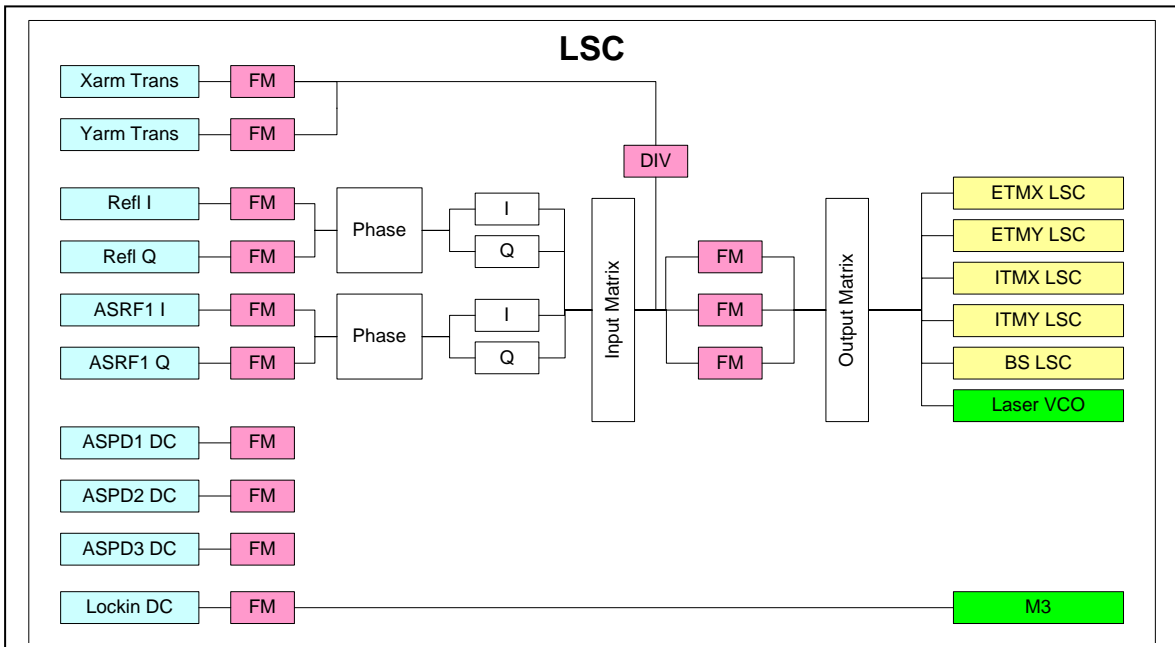
In addition, four DC offset adjustments are provided to the pitch and yaw inputs of the PZT drivers for M1 and M2. These are manual adjustments only.



### 6.3 LSC Software

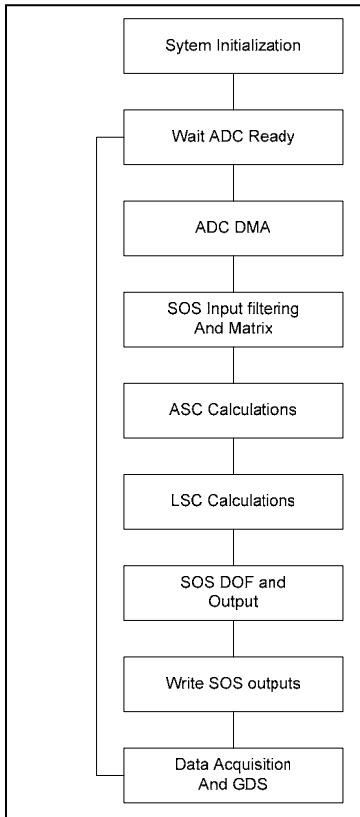
A code diagram for the LSC is shown in the figure below. Two RF photodiode inputs are phase corrected and applied to an input matrix. The two transmitted light monitors are used after the input matrix to normalize the RFPD signals prior to application of the signals to three DOF filter modules. The outputs are then applied via software to all suspension LSC inputs and as a DAC signals to the PSL..

In addition, three ASPD DC signals are acquired for data acquisition only. A fourth DC signal, the Lock In signal, is input for direct application to M3 via a DAC output.



## 6.4 Software Control Flow and Partitioning

The previous subsections described the software for the individual components to be controlled. This code must still be constructed to run in the proper sequence to integrate these components, particularly where ASC and LSC control calculations feed into the SOS controls. The figure to the left shows the basic code sequence, which is to run in a loop at 64KHz initially, with a path to 128KHz later.



- Wait ADC Ready: The software is timed by the ADC, which is in turn clocked from the Lasti timing system at 64KHz. The front end code is idle while waiting for a sample to be ready.
- Once ready, the ADC data is acquired by use of the ADC DMA facility.
- All SOS input filtering and input matrix calculations are performed.
- All ASC calculations are performed.
- All LSC calculations are performed.
- The SOS DOF filter calculations are performed, with LSC and ASC calculations, along with all SOS outputs filtering.
- SOS control outputs are sent via DAC channels.
- All 'housekeeping' functions are performed, which includes all data acquisition and GDS functions.
- Code returns to wait for next ADC sample set.

## 7 Implementation Plan

A development and test system is available at Caltech with all of the hardware components necessary to begin code development and early testing of key system features. The plan is to make use of this equipment and proceed roughly as follows:

- Code in the software blocks described previously for the SOS controls, ASC and LSC.
- Initially run the software at 64KHz on a dual Opteron computer to get preliminary timing benchmarks. If the code proves to run with a comfortable margin, this may be the first system shipped to MIT.
- Continue testing at 128KHz. If initial dual Opteron timing tests fail at this rate (or at 64KHz), move to restructuring the code to run on a quad CPU platform.
- Order the Lasti hardware. This should be done no later than early April to make an early summer delivery.
- Deliver system to MIT for installation and initial testing (June 2006).

## 8 Cost Estimate

A cost estimate for the Ponderomotive CDS digital components is given in the following table. The greatest uncertainty at this time is the cost of the computer. The present cost of a quad Opteron computer is shown. The spring season often brings about matching grant discounts, which could drop the price to about \$10,000. On the other hand, test results may show that a more powerful machine may be required, driving costs in the other direction.

<b>Ponderomotive CDS Cost Estimate (Digital controls portion only)</b>			
<b>Description</b>	<b>QTY</b>	<b>Unit Price</b>	<b>Total</b>
Quad AMD64 Computer	1	\$12000	\$12000
ADC Module	2	\$4000	\$8000
DAC Module	2	\$3500	\$7000
MyriNet NIC	1	\$550	\$550
Digital I/O Module	2	\$300	\$600
<b>TOTAL COST</b>			<b>\$28,150</b>