

LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

CALIFORNIA INSTITUTE OF TECHNOLOGY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	DCC Number	February 8, 2006
	DRAFT	
Lasti Ponderomotive Experiment Digital Controls Design		
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1 Scope

The scope of this document is the digital controls design for the CDS control and monitoring of the Lasti Ponderomotive Experiment. Covered in this scope are all of the analog to digital convertors required and their connection interfaces, computers and software, and digital connections to the Lasti CDS infrastructure. Specifically excluded are any analog signal conditioning units required and field cabling to the sensors and actuators (covered under separate documentation).

2 Purpose

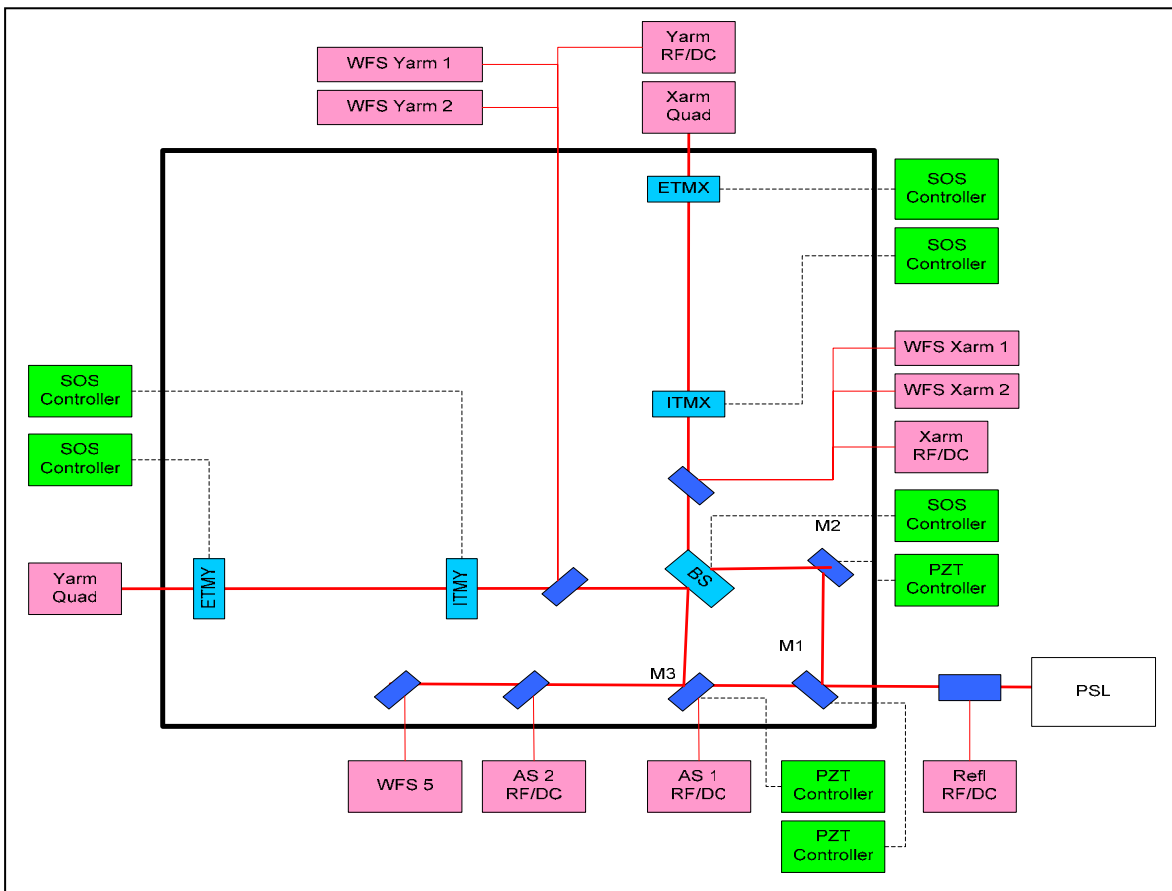
The purpose of this document is to describe a CDS design for the digital hardware and software required to control and monitor the Lasti Ponderomotive experiment.

3 References

1) LIGO T060031-00-C LASTI Digital Control and Data System (CDS) Design

4 Overview

Over the course of the next year, a Ponderomotive experiment will be conducted at the Lasti facility. An overview of the experiment components and layout are shown in the following figure..



To support this effort, CDS equipment will be provided, with installation to begin in the summer of 2006. As indicated by the diagram, the CDS must provide for control, monitoring and integration of several components:

- Suspended Optics Controls: Five small optic suspension (SOS) controllers will be provided, similar to the present Ligo SOS controllers.
- Alignment Sensing and Control: Five WaveFront Sensors (WFS) and two Quad Photo Diodes (QPD) are to be used to present alignment information.
- Length Sensing and Control (LSC): A total of five RF photodiodes will provide for length sensing.

As part of the requirements, many of the control loops involved in this system must run at 64KHz. In the design reflected in this document, all loops will run at 64KHz. There is one exception. There is a desire to run a feedback loop to the PSL at 500KHz and that this be done digitally. Further requirement specifications, necessary to make a final design decision, are still TBD.

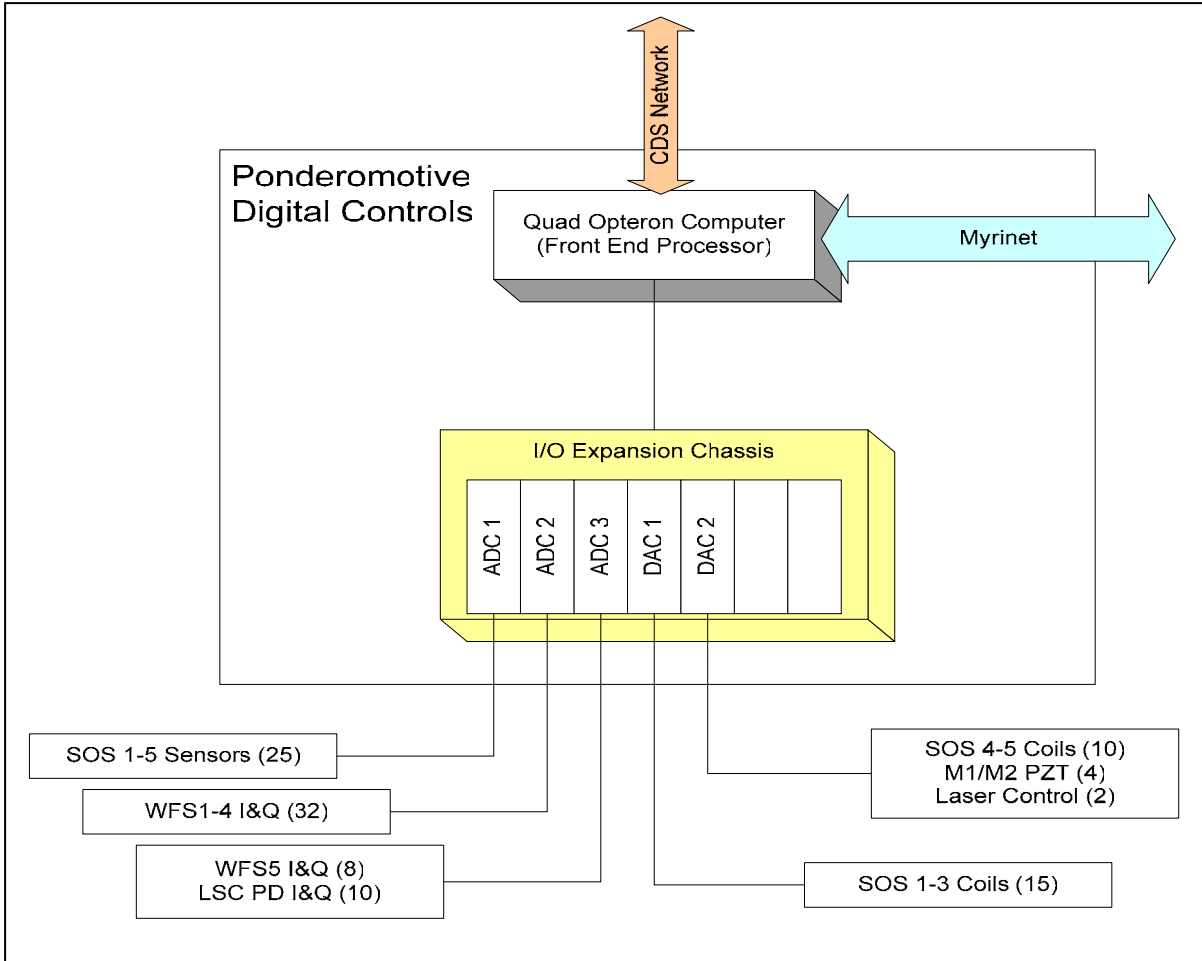
5 CDS Hardware

The CDS hardware implementation will follow the PCI design concepts for Lasti described in Reference 1. The specific digital hardware components for this CDS subsystem include:

- One quad AMD64 (Opteron) computer
- One PCI-X expander chassis
- Three ADC modules
- Two DAC modules
- One MyriNet Network Interface Card (NIC)

A sketch of the Ponderomotive control components and their interconnection are shown in the following figure. Note that the signal count is based on the number of Ligo connections for similar components. However, both I&Q phase signals from ISC sensors may not be required, which would reduce the channel count.

Five of the seven available slots of the PCI-X expansion chassis are accounted for here. If the 500KHz loop is implemented digitally, then the remaining two slots may be occupied by high speed (2M sample/sec) ADC and/or DAC modules.



5.1 Analog Signal Connections

Analog signals will be connected to the digital I/O modules via cabling from the analog signal conditioning units. The signal connections to the ADC and DAC modules are given in the following tables. Along with the signals listed, timing clocks from the Lasti timing system will also be provided to all ADC/DAC modules via the analog conditioning units. *Note that this signal list is preliminary and provided at this time primarily for channel counting purposes.*

ADC MODULE 1 – SOS Sensor Signals			
Ch.	Signal	Ch.	Signal
00	ETMX UL Sensor	16	ETMY UL Sensor
01	ETMX UR Sensor	17	ETMY UR Sensor
02	ETMX LL Sensor	18	ETMY LL Sensor
03	ETMX LR Sensor	19	ETMY LR Sensor
04	ETMX Side Sensor	20	ETMY Side Sensor
05	ITMX UL Sensor	21	ITMY UL Sensor
06	ITMX UR Sensor	22	ITMY UR Sensor
07	ITMX LL Sensor	23	ITMY LL Sensor
08	ITMX LR Sensor	24	ITMY LR Sensor
09	ITMX Side Sensor	25	ITMY Side Sensor

10	BS UL Sensor	26	NC
11	BS UR Sensor	27	NC
12	BS LL Sensor	28	NC
13	BS LR Sensor	29	NC
14	BS Side Sensor	30	NC
15	NC	31	One PPS Timing Signal

ADC MODULE 2 – WFS1 thru WFS4 Signals			
Ch.	Signal	Ch.	Signal
00	WFS1 I1	16	WFS2 I1
01	WFS1 I2	17	WFS2 I2
02	WFS1 I3	18	WFS2 I3
03	WFS1 I4	19	WFS2 I4
04	WFS1 Q1	20	WFS2 Q1
05	WFS1 Q2	21	WFS2 Q2
06	WFS1 Q3	22	WFS2 Q3
07	WFS1 Q4	23	WFS2 Q4
08	WFS3 I1	24	WFS4 I1
09	WFS3 I2	25	WFS4 I2
10	WFS3 I3	26	WFS4 I3
11	WFS3 I4	27	WFS4 I4
12	WFS3 Q1	28	WFS4 Q1
13	WFS3 Q2	29	WFS4 Q2
14	WFS3 Q3	30	WFS4 Q3
15	WFS3 Q4	31	WFS4 Q4

ADC MODULE 3 – WFS5 and LSC Sensor Signals			
Ch.	Signal	Ch.	Signal
00	WFS5 I1	16	ASPD1 I
01	WFS5 I2	17	ASPD1 Q
02	WFS5 I3	18	ASPD2 I
03	WFS5 I4	19	ASPD2 Q
04	WFS5 Q1	20	Xarm PD I
05	WFS5 Q2	21	Xarm PD Q
06	WFS5 Q3	22	Yarm PD I
07	WFS5 Q4	23	Yarm PD Q
08	NC	24	REFL PD I
09	NC	25	REFL PD Q
10	NC	26	NC
11	NC	27	NC
12	NC	28	NC
13	NC	29	NC
14	NC	30	NC
15	NC	31	NC

DAC MODULE 1 – ETMX, ETMY, BS Coil Drives			
Ch.	Signal	Ch.	Signal
00	ETMX UL Coil	08	ETMY LR Coil
01	ETMX UR Coil	09	ETMY Side Coil
02	ETMX LL Coil	10	NC
03	ETMX LR Coil	11	BS UL Coil

04	ETMX Side Coil	12	BS UR Coil
05	ETMY UL Coil	13	BS LL Coil
06	ETMY UR Coil	14	BS LR Coil
07	ETMY LL Coil	15	BS Side Coil

DAC MODULE 2			
Ch.	Signal	Ch.	Signal
00	ITMX UL Coil	08	ITMY LR Coil
01	ITMX UR Coil	09	ITMY Side Coil
02	ITMX LL Coil	10	M1 PZT Pitch
03	ITMX LR Coil	11	M1 PZT Yaw
04	ITMX Side Coil	12	M2 PZT Pitch
05	ITMY UL Coil	13	M2 PZT Yaw
06	ITMY UR Coil	14	Laser Control (ASC)
07	ITMY LL Coil	15	Laser Control (LSC)

5.2 Digital Signal Connections

Two digital signal paths exist to/from the front end control computer. All realtime network traffic, including data acquisition, is routed through the CDS Myrinet fabric. The front end computer will be connected to this network via a pair of multi-mode fiber optic cables.

Data acquisition and storage will be provided by the Lasti FrameBuilder. For purposes of connection within the Lasti DAQ system, this front end computer will be designated with a Data Collection Unit Identification (DCUID) number of 11.

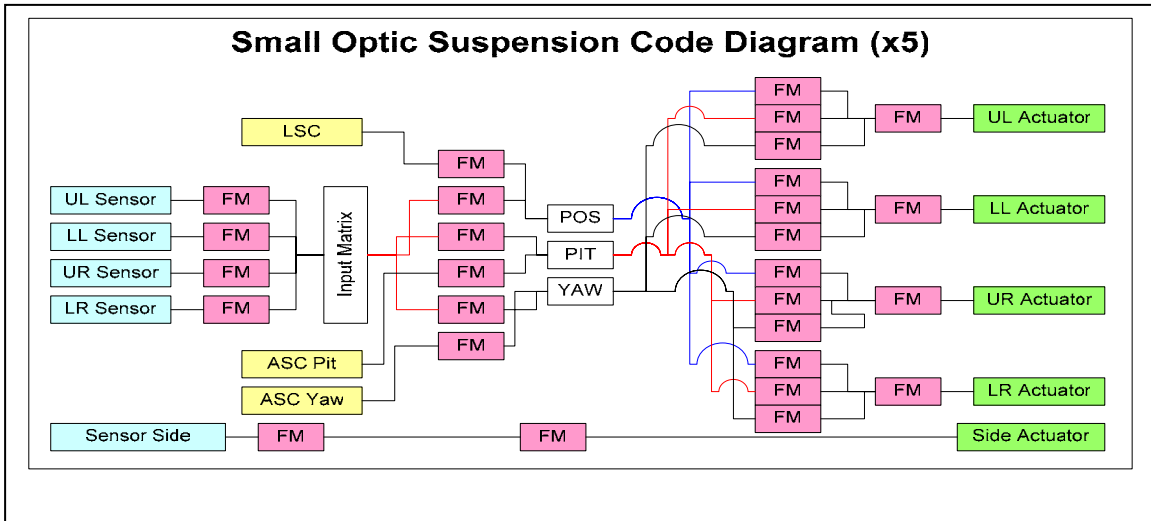
For transmission of EPICS data and other non-realtime communications, the front computer will be connected to the Lasti CDS Ethernet. This is a 100baseT copper wire connection via an RJ45 connector.

6 Software

The Ponderomotive front end control software will make use of the basic control code libraries developed for PCI based systems, as further described in Reference 1. It will also make use of CDS standard components previously developed for Ligo controls, such as the CDS standard IIR filter module.

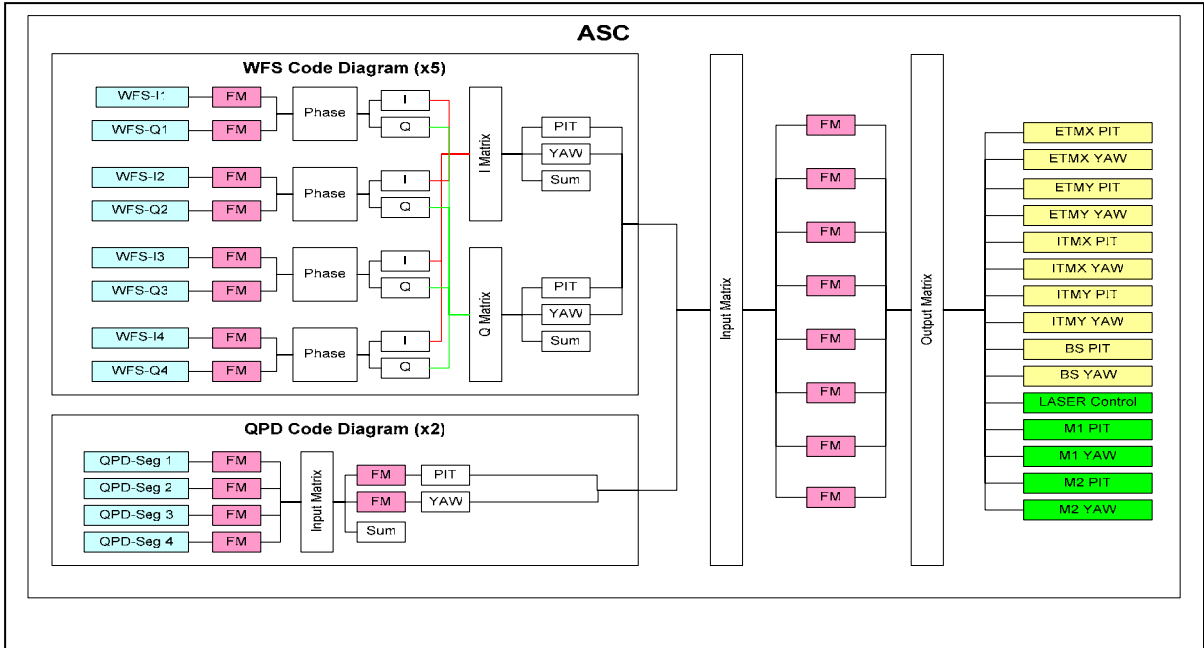
6.1 Small Optics Control Software

It is intended that the SOS control software be identical to that used in Ligo. A block diagram of that software is shown in the figure below. This code block is replicated five times for the five SOS controllers. Note that in this diagram, and others that follow, that ADC inputs are shown in blue, DAC outputs in green and internal software connections in yellow.



6.2 ASC Software

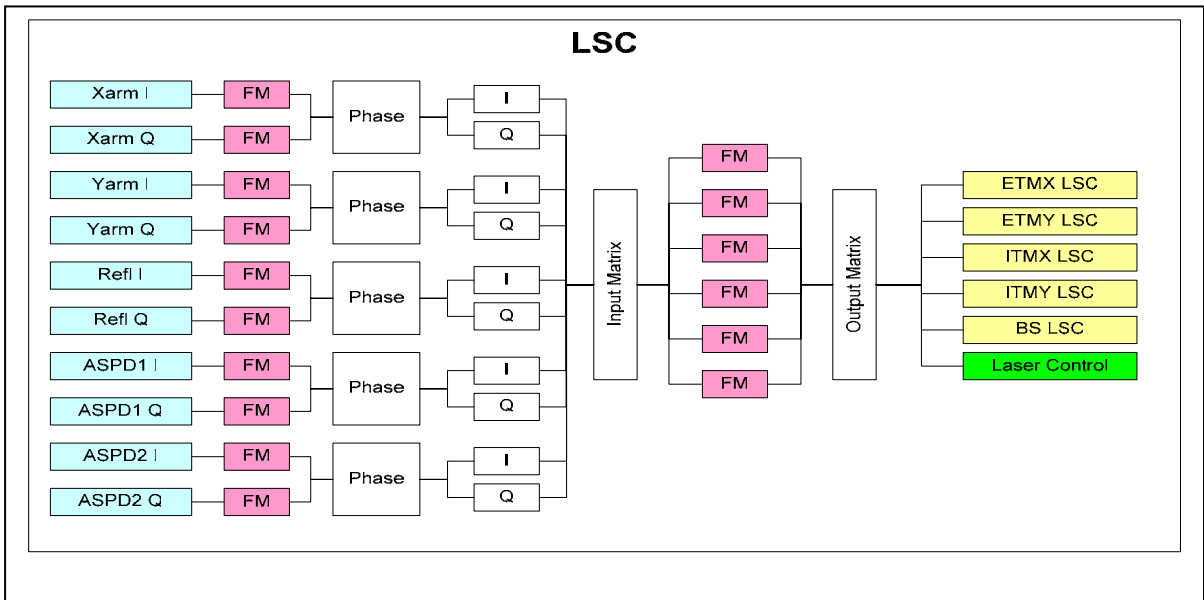
The software for the ASC portion of control is again similar to that of Ligo ASC systems. A basic block diagram is shown in the following figure. It consists of five identical WFS input section code blocks and two identical QPD input section code blocks. The outputs of the WFS and QPD sections feed an input matrix, which fans out to TBD degree of freedom (DOF) filter modules. The DOF filters feed an output matrix and then the various actuator points.



6.3 LSC Software

The basic filtering algorithm for the LSC is shown in the figure below. Again, this is similar to the Ligo implementation. The exact number of DOF filters is still TBD.

A key component to a final design is the desired IFO locking scheme, which is still TBD.



6.4 Software Control Flow and Partitioning

The previous subsections described the software for the individual components to be controlled. This code must still be constructed to run in the proper sequence to integrate these components, particularly where ASC and LSC control calculations feed into the SOS controls. Before this can be done, the aforementioned TBD LSC locking scheme must be understood. Once that design is ready, then the code sequencing scheme can be implemented.

The last piece will be to partition the code operations between the multiple processors that are available in the front end computer, such that the timing and sequencing are correct to complete all operations for one control cycle in $\sim 15\mu\text{sec}$.

7 Implementation Plan

A development and test system is available at Caltech with all of the hardware components necessary to begin code development and early testing of key system features. The plan is to make use of this equipment and proceed roughly as follows:

- Code in the known software blocks described previously for the SOS controls, ASC and LSC.
- Provide a generic mechanism to divide and synchronize this code between 3 of the 4 Opteron processors available in the front end computer (fourth CPU is used for non-realtime applications, such as EPICS, GDS functions).
- Run this base code at 64KHz (65536Hz) and get preliminary timing and loading information.
- Incorporate a baseline design for an LSC locking scheme.
- Continue timing and performance testing to determine the final computer configuration required to run comfortably at 64KHz.
- Order the Lasti hardware. This should be done no later than early April to make an early summer delivery.
- Deliver system to MIT for installation and initial testing (June 2006).

There will also be some studies done on the feasibility of running a PSL control loop at 500KHz. Some initial testing is looking favorable. A loop with 8 ADC inputs, 8 filter modules, and 8 DAC outputs has been run on the development system with a cycle time of $\sim 1.5\mu\text{sec}$. However, better specifications of the PSL loop are required prior to performing further tests and come to a final conclusion.

8 Cost Estimate

A cost estimate for the Ponderomotive CDS digital components is given in the following table. The greatest uncertainty at this time is the cost of the computer. The present cost of a quad Opteron computer is shown. The spring season often brings about matching grant discounts, which could drop the price to about \$10,000. On the other hand, test results may show that a more powerful machine may be required, driving costs in the other direction. Also, this estimate does not yet include any additional hardware required for a possible 500KHz PSL control loop (additional \$4K to \$8K).

Ponderomotive CDS Cost Estimate (Digital controls portion only)			
Description	QTY	Unit Price	Total
Quad AMD64 Computer	1	\$14000	\$14000
PCI-X Expander	1	\$3100	\$3100
ADC Module	3	\$4000	\$12000
DAC Module	2	\$3500	\$7000
MyriNet NIC	1	\$550	\$550
TOTAL COST			\$36,650