

## Direct Digital Down-Conversion for LIGO Wavefront Sensors, SURF Progress Report 1 ( 6/23/2003 )

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### 1. INTRODUCTION

Currently, photodiode sensor systems in LIGO utilize analog demodulation systems. While these systems provide the time-tested reliability as well as nearly instantaneous response times that are associated with analog systems, they fall short in terms of flexibility. For each application, we must design a different analog circuit, and in turn, produce a different circuit board. In addition, analog systems limit the feasibility of designing high-Q filters at low frequencies due to component number and size. As number of analog components increase, thermal noise increases as well.

In order to improve system flexibility, we are seeking to implement digital demodulation systems as replacements for the analog systems currently found in the wavefront sensors and other similar photodiode detector systems. Digital systems provide clear advantages in flexibility and filter design, as well as a potential advantage in noise immunity. We can create a single hardware design that can simply be reprogrammed according to the system's desired application. Additionally, we can implement in software any filter that can be mathematically described, regardless of order or frequency. In the area of system noise, a digital system could outperform an analog system. When we initially digitize the incoming signal, we introduce noise; in the rest of the system, we control the amount of noise by specifying the number of bits we will carry through calculations. With a good ADC and enough bits, we hope to at least match the noise immunity of an equivalent analog system.

Where digital systems falter is in response time. Since incoming signals must be digitized, then passed through logic and multiplication circuits that are governed by a system clock, we observe considerably more latency in digital systems than in analog systems. While many devices in industry use digital demodulation, their performance is not acceptable for LIGO applications. For example, mobile phones and digital FM radio receivers use digital demodulators with latencies in the range of a few milliseconds. While this is acceptable in such applications, the servos in LIGO require latencies smaller than 10 to 100 microseconds in order to maintain the stability of alignment and calibration systems.

### 2. RESEARCH AND METHODS

My project focuses on designing a proof-of-concept device, which will serve as a stepping-stone towards replacing the analog demodulation systems with programmable digital systems, especially for Advanced LIGO. While my mentor, Jay Heefner, believes that we can achieve acceptable, or even superior, performance with digital systems, it has not been proven by demonstration of a working system. I have the responsibility of doing preliminary work and demonstrating that such a system can meet performance requirements.

For my research, I will be using a Stratix DSP Development Kit from Altera. The Stratix Kit comes packaged with all software necessary, including Matlab, Simulink,

Altera DSP Builder, and Quartus II. The Altera Stratix chip is an FPGA with integrated DSP capabilities. While we anticipate this chip to have capabilities far exceeding our application, the convenience and price of the Development Kit makes it a great place to start.

To successfully demonstrate an acceptable digital demodulator, I will need to research the following areas:

- Noise as a result of analog to digital conversion
- Latency of FIR vs. IIR filter designs
- Undersampling
- Downsampling and decimation
- Aliasing
- VHDL.

My first goal was to build a simple demodulator without accounting for any performance optimizations. This would give a baseline of worst-case performance by which we can observe the effectiveness of detailed design considerations in the above areas.

### **3. CURRENT PROGRESS AND GOALS**

After receiving the Stratix DSP Development Kit, I followed a simple tutorial that demonstrated the use of DSP Builder to program the Development Board. DSP Builder allows synthesis of FPGA and DSP designs directly from a Simulink model without having to write VHDL code. While this is extremely useful in quickly designing a functional system, I expect to have to write VHDL in order to optimize portions of a proof-of-concept design that will be useful for LIGO.

Currently, I have used DSP Builder to implement a working demodulator for amplitude-modulated signals. Although my initial design is relatively crude, its performance suggests that we will be able to design a demodulator suitable for use in LIGO. *Table 1* shows performance characteristics of the initial demodulator design with sinusoidal and square-wave modulation. This demodulator uses an 80 MHz clock for all ADCs, DACs, and logic. Because the 15 MHz carrier is well below the Nyquist frequency (40 MHz for this setup), the demodulator should have no aliasing problems. When increasing the carrier frequency above the Nyquist frequency, we should band-limit the signal to a bandwidth less than the Nyquist frequency before sending it into the ADC. Because we did not do this, we observed aliasing at various frequencies above 40 MHz. We randomly chose to try a 200 MHz carrier, but we observed aliasing. By changing the carrier frequency in 1-MHz increments, we were able to find a “sweet-spot” at 207 MHz where we observe no aliasing, even though we did not band-limit the carrier.

**Table 1. Demodulator performance with amplitude modulation.**

Carrier Frequency	Modulation	Noise Floor, dB <sub>rms</sub> /√Hz	Latency, μs
15 MHz	Sinusoidal	-135	–
207 MHz	Sinusoidal	-140	–
15 MHz	Square	-130	2
207 MHz	Square	-135	2

For the next month, my goal is to design a working I-Q demodulator and successfully test it in the Pre-Mode Cleaner at Caltech's 40-meter interferometer. In order to do this, I will need to:

- Create my own IIR and FIR filters instead of using the blocks in DSP Builder
- Design an I-Q demodulation algorithm
- Build an analog anti-aliasing filter for the system input.

I will measure success by whether or not the Pre-Mode Cleaner can lock using my digital design as a replacement for the analog demodulator currently used.

#### 4. CHALLENGES

In the last month, the greatest challenges have been acquiring the proper licenses for and learning the quirks of the software. After talking with Altera technical support twice, I finally received the licenses and set up the software. The software has made it relatively easy to implement a design on the development board, but it does have some occasional quirks. For example, the FIR filter IP core used in DSP Builder does not always compile. In order for a design using an FIR to compile properly, I have to copy the FIR filter files from an example tutorial to my project and rename them with my project name. After doing this, I can then edit the FIR in any way and it compiles properly.

Compile times are also a trying issue. Compiling a project from DSP Builder includes automated project analysis and synthesis, as well as fitting. While easy to do, compiling can take about an hour on my 3-GHz computer. Maximum compile times occur when using an FIR filter IP core in the design; otherwise, compilation is on the order of 5 to 10 minutes. This is a challenge because I essentially get 1 chance per hour to test my design. I hope to overcome this by learning to program my own FIR algorithms, which will hopefully decrease compile times.

For the next month, I anticipate my greatest challenges to be in learning to program my own filter algorithms and in programming an I-Q demodulator. These two things should be everything I will need to use in order to verify the operation of a working digital demodulator.

**5. RESOURCES**

I have access to most resources that I should require in order to complete my project, including articles published by the IEEE, textbooks from my mentor and the library, and a test setup on my desk. The only resource that I do not have is an experienced person that can help me learn VHDL and DSP. Instead, I must rely on textbooks, tutorials, and online articles in order to learn these skills. While not the most time-efficient means of learning, I have confidence that I can effectively use the resources I have.