

LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
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Ultra Low Noise VGA		
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Design Ideas*

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Ultra Low Noise VGA

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There are a number of single chip variable gain amplifiers (VGAs) on the market today. Unfortunately they all have drawbacks such as high noise, ± 5 volt limit, low input impedance or nonlinear gain/frequency characteristics. The circuit in **figure 1** is a 16 step ultra low noise VGA that solves many one these problems. IC1 is a low noise quad op amp and IC2 is a quad SPDT CMOS switch. The stages are arranged to switch in successive multiplication factors using a TTL binary code. The values shown provide 0 to 45 dB gain in 3 dB steps. For best low noise performance the higher gain stages are placed in front of lower gain stages. The circuit as shown exhibits about 3nV/rt-Hz noise referred to the input (RTI) at most gain settings. The highest noise is 4.5nV/rt-Hz (RTI) at a gain of 9 dB. Distributing the total gain across multiple stages has the advantage of increasing the overall bandwidth. The output stage is configured differently so that there is a low impedance output driver at all gain settings.

If the gain needs to be controlled remotely one must be concerned about ground loops that can compromise the low noise characteristics of the circuit. One solution is to place opto isolators on the four digital control lines so that no ground connection exists between that two ends of the cable except through the power supply. The solution used here is an analog differential control voltage with an ADC to generate the four bits. **Figure 2** shows a circuit that performs this function quite well. IC3 is a differential receiver and IC4 is an 8-bit ADC. In some application one could get away with just using the ADC since it already has a differential input. However, care must be taken not to exceed the narrow common mode range of the ADC input. A more robust solution is to place a differential receiver in front of the ADC as shown. R11 and C7 form a low pass filter for the control voltage into the ADC. The high order 4 bits out of the ADC are used to control the CMOS switches. As shown the ADC operates in a self clocking mode and needs no other controls. The frequency of the sampling is controlled by R9 and C7 and is about 640KHz for the values shown. D3, R13 and C9 form a power up initialization for the ADC clocking function.

Step	Gain		Noise (RTI) nV/rt-Hz	3 dB BW (MHz)
	dB	V/V		
0	0	1.0	3.1	10.5
1	3	1.4	3.8	7.7
2	6	2.0	4.4	5.1
3	9	2.8	4.5	4.6
4	12	4.0	3.6	2.7
5	15	5.6	3.6	2.7
6	18	7.9	3.7	2.6
7	21	11.2	3.7	2.6
8	24	15.8	3.0	0.88
9	27	22.4	3.0	0.89
10	30	31.6	3.0	0.94
11	33	44.7	3.0	0.96
12	36	63.1	3.0	0.97
13	39	89.1	3.0	0.97
14	42	125.9	3.0	1.04
15	45	177.8	3.0	1.02

Table 1

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The control voltage steps are 310 mV apart providing plenty of noise immunity. **Table 1** shows the performance of the overall circuit with analog control. R9 and R10 in **Figure 1** can be used to shift the overall gain range down with very little sacrifice of noise characteristics.

Ideas for further enhancements:

The individual gain stages can obviously be chosen to give other ranges and step sizes such as 0 to 30 dB in 2 dB steps. At the expense of circuit simplicity the quad op amp could be replaced with four ultra low noise op amps such as the LT1128 or AD797. This will lower the RTI noise to about 1.4nV/rt-Hz. The number of stages can be increased providing either a wider dynamic range or finer gain steps or both.

The benefits of this circuit over commercially available single chip VGAs include ultra low noise, ± 13 volt range, high bandwidth, high input impedance, ground loop immunity, low cost and user defined dynamic range and step size.

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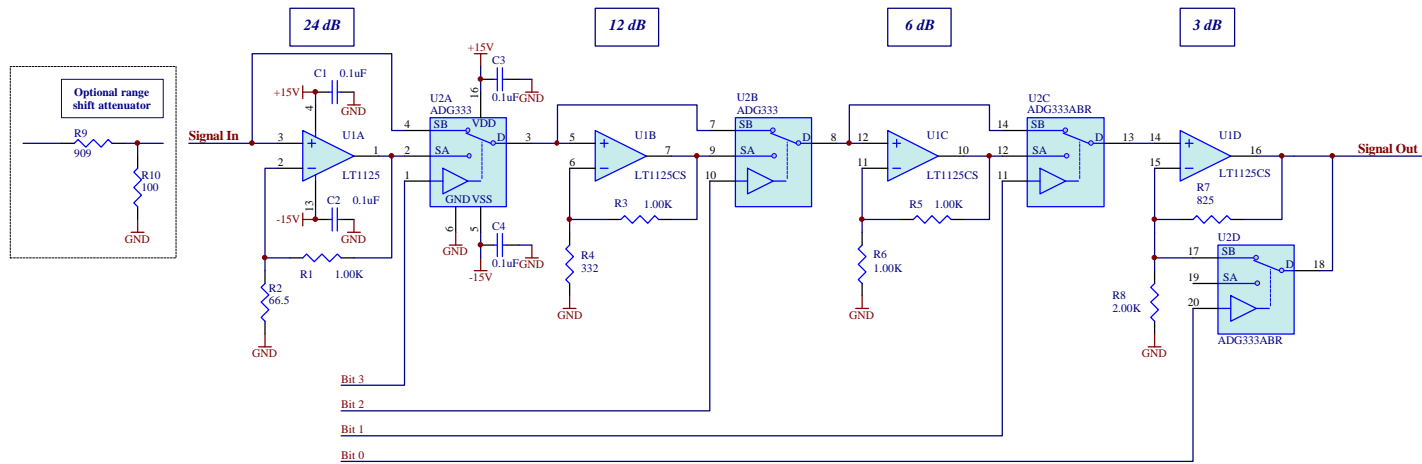


Figure 1

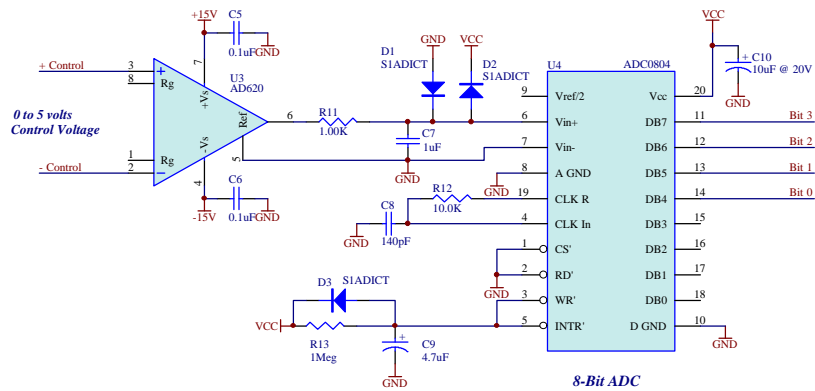


Figure 2

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